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New varactors and high-power high-frequency capacitive devices

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Abstract

A new class of semiconductor devices is proposed with electrically controlled electrode's area. It is shown that by implementing this basic idea within the commonly available technology one is able to construct the varactors (varicaps) with almost any prescribed C-U characteristic in contrast to severely limited functionality of traditional devices. More importantly, very promising new devices (which we call Semiconductor Intelligent Capacitances -SICs) can be produced using these varactors. In contrast to known semiconductor devices SICs are able to overcome the fundamental electronic constraint on the maximum power handling capability, which is currently a real stumbling block for any semiconductor device due to final velocity of mobile charge carriers and junction breakdown. SIC-based ultra-high power frequency transducers and capacitive transformers can be easily fabricated by means of standard planar technology and are expected to replace bulky inductive transformers in high-frequency and microwave integrated circuits. Also described are some 'proof-of-the-concept' experiments performed by the authors. Results obtained are very encouraging.

Key words: varactor, frequency multiplication, parametric amplifier

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1. Instead of introduction

Instead of lengthy introduction, wherein one is expected to demonstrate an acquaintance with (at least) the most important previous work in the same or related subject, we prefer to proceed directly to the point. Every schoolchildren knows that capacitance of parallel-plate capacitor (ignoring edge effects, which can be quite important in some cases, especially when the capacitor is small) is given by very simple relation:

$$C = \frac{\varepsilon_0 \varepsilon S}{d} \tag{1.1}$$

where ε_0 =8.85x10^{-12} F/m is the vacuum dielectric constant, ε(T, P, E, ω) is the dielectric function of the insulator separating the capacitor's plates (it's dependence on temperature T, pressure P, electric field strength E and frequency ω is explicitly indicated), S is the area of the plates and d is the distance between them.

As can be seen from (1.1) there are only three options for getting a variable capacitance:

(a) by varying ε, if, for example, use is made of the functional dependence $\varepsilon = f(E)$, where electric field strength in the insulator is given by $E = \frac{U}{d}$, U being the voltage applied between plates;

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(b) by changing electrode's area S , for example, by simply sliding the plates against each other, in which case S will designate the overlapped area;

(c) by varying the distance d between plates.

As a matter of fact, only the third option (variable d) is widely exploited in present day microelectronics using all three its basic building blocks, i.e., p-n junctions, metal-insulator-semiconductor (MIS) structures, and Schottky barriers. Under appropriate bias conditions in all these devices a space-charge region (SCR) is formed, which is almost exactly analogous to insulator in usual capacitor, the only difference being that SCR width, d , is controlled by the voltage applied, $d = d(U)$.

The effect is known for quite some time and is excellently reviewed in a number of books both from physical point of view [1-3] as well as circuit applications [4]. The shortcomings of any traditional varactor with standard design are well known and seem almost insurmountable. It is widely believed that it is impossible to realize an *arbitrary predetermined* $C(U)$ characteristic because of technological constraints preclude the opportunity to get a predetermined impurity distribution in the body of the device. It is also known that one is unable to realize some practically important $C(U)$ characteristics (for example, *linear*) by means of any impurity distribution within the device body

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achievable in real practice. It is also evident that a minimum value of varicap capacitance is almost always determined by the breakdown voltage of the junction used, putting thus a fundamental limit on the magnitude of $C_{\min}$.

Our purpose here is to show how these limitations can be removed and to this end in the present work we will show how to make semiconductor capacitances with electrically controlled electrode's area [5], thus adding new and important dimension for device design and implementation.

Most easily one of the ideas behind our approach can be understood with reference to Fig.1, which shows a cross-section of a wedge-shaped uniformly doped piece of a semiconductor with two Schottky barriers (or homo- or hetero-p-n junctions or MIS structures, as the case may be [6]) formed on its top and bottom surfaces. Also shown in Fig.1 is the extension of space-charge region under increasing reverse bias. One can see immediately that for this non-parallel plate semiconductor capacitor the effective area of electrodes shrinks progressively under the influence of reverse bias, i.e. we have not only $d = d(U)$, but also $S = S(U)$. This is a *key point* as will become clear below. We, however, would like to warn the reader right from the beginning that in some cases there is no need for wedge-shaped samples or samples with lateral impurity gradients for implementation of the

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central idea (**SIC**) to be described in section 3. The present article is organized as follows. In the next two chapters the principles of operation and some basic implementations are presented for new varactors demonstrating that (in contrast to traditional one's) it is technologically feasible to get almost any desired $C-U$ with very high $C_{\max}/C_{\min}$ ratio. Simple technological methods for obtaining these varactors are described in part 4. In chapter 3 some possible applications of new capacitive devices are discussed with emphasis on their advantages as compared to other semiconductor devices used for the same purposes. Our aim here is to explain in simple terms the operational principles and practical ways of fabrication of these new devices. Due to somewhat nonstandard extent of the article the experimental data are invoked only when it was necessary.

2. Varicaps with prescribed capacitance-voltage characteristics

2.1 Linear varicaps

Obviously, the wedge-shaped samples are not very convenient for planar technology. Fortunately, the basic principle can be easily reformulated and applied within the standard planar mainstream. Fig.2 shows one possible implementation. On p^+-substrate with back ohmic contact a thin low-doped n-layer is grown with a thickness D. In the active region of the device (defined by $0 \le x \le x_{\max}, 0 \le z \le F(x)$) a nonuniform donor profile

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$N_i(x,y)$ is generated using, for example, ion implantation, so that impurity concentration (dose) increases from $x_{\max}$ toward the origin of indicated coordinate system. Active region is supplied by top ohmic contact on its periphery. Outside active area the film thickness and doping level are chosen so that n-type film is fully depleted by majority charge carriers. Upon application of reverse bias to film-substrate n-p^+ junction the space-charge region (SCR) gradually fills the active volume of the device. Then, both the size of neutral region, $H(U)$, along x-coordinate and effective area, S, of capacitor plate decrease continuously since

$$S = \int_0^{H(U)} F(x)dx + S_{cont} \qquad (2.1)$$

where S_{cont} is the area of the top ohmic contact including contact pad. Now, to obtain the desired $C(U)$ characteristic we have at our disposal two *functions* $F(x)$ and $N_i(x,y)$, which can be varied separately or together, in sharp contrast to conventional varactors whose $C(U)$ depends only on $N_i(x,y)$. In this way we are able to replace a rather intricate technical problem of generating strictly specified impurity distribution within the device body by much simpler task of fabrication of a surface mask with a precalculated shape.

Let $d(x,U)$ be the width of SCR at some location x when reverse bias is U (see Fig.2). Then $d(x,U)$ is given (through double integration of Poisson equation) by

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$$U + U_{bi} = \frac{q}{\varepsilon\varepsilon_0} \int_0^{d(x,U)} y N_i(x,y)\,dy \qquad (2.2)$$

where U_{bi} is the built-in potential of p^+-n junction whose dependence on x through $N_i(x,y)$ is here ignored (being almost negligible), and ε is the dielectric constant of semiconductor. Then, obviously (cf. Fig.2), $H(U)$ can be calculated from

$$d(x,U) = D \qquad (2.3)$$

and finally we get for $C(U)$ characteristic of the device

$$C(U) = \varepsilon\varepsilon_0 \int_0^{H(U)} \frac{F(x)}{d(x,U)}\,dx \qquad (2.4)$$

Using equations (2.2)-(2.4) one can easily calculate the *lateral shape* $F(x)$ (i.e. masking pattern) of the active region for almost *any* prescribed $C(U)$ with almost *any* $N_i(x,y)$ within active volume of the device. This, apparently missed extra degree of freedom, is of great importance for the whole range of varactor applications.

But first of all, we would like to consider varicaps with *strictly linear* $C-U$ characteristics *over all working* range of applied biases (varicaps with *approximately linear* $C(U)$ characteristics for a *limited range* of reverse biases are known for more than 40 years [4]). As a matter of fact, it can be shown analytically that for clino-varicaps the linear C-U characteristic can be obtained only for about 66% of their working bias range.

As is well known, for frequency multiplication [4] and parametric amplification [7] *linear* varactors are indispensable, simply because for these devices the average capacitance is independent on the amplitude of harmonic signal. As a result, there is no detuning in resonant circuits *if* (nonexistent up to now) *truly linear* varicaps are used. The same useful property is obtained for varicaps with symmetrical C(U) characteristic

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(see e.g., ref. [8-10]), but, nonetheless, linear varicaps are preferential in some applications.

Fig.3 presents specific example of the active area shaping[1] for linear varactor fabricated by phosphorus ion implantation (E=200 keV) into high-purity Si film (0.6 μm thick) with linearly increasing (along x) dose from 1.5×10^{11} ions/cm^2 at $x = x_{\max}$ to 1.0×10^{12} ions/cm^2 at $x = 0$ (see Fig.2). The layer is grown on degenerately boron-doped ($p^+ = 10^{20}$ cm^{-3}) substrate (the built-in voltage was taken to be $U_{bi} = 0.6\ V$ everywhere in the active region).

Device shown in Fig.2 has an obvious disadvantage, namely, a rather low figure of merit due to large series resistance of neutral volume. It can be, however, eliminated by simply providing on the surface of active region a set of high-conductivity strips along z direction as shown in Fig.4 [12].

The quality factor Q for varactor without strips (Fig.2) can be estimated (neglecting reverse current of a p^+-n junction) as a ratio of varactor's capacitive resistance to undepleted volume series resistance

$$Q = \frac{1}{\omega CR} \tag{2.5}$$

where ω is the angular frequency of the driving voltage. If ρ_{av} is the average specific resistivity of the neutral part of the active volume and F_{av} is the average value of $F(x)$ over the $0 \le x \le H(U)$ interval than for $H(U) \gg F_{av}$ we have

$$R \approx \frac{F_{av}\rho_{av}}{DH(U)} \tag{2.6}$$

and

[1] Idea of shaping of the active volume of the varicap in order to obtain something useful in its C-U characteristic is by no means new. See, for example, ref.[11] where 'pagoda'-shaped varactors are described. Our approach, however, is much more powerful being planar at the same time.

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$$C \approx \frac{\varepsilon\varepsilon_0 (F_{av} H(U) + S_{cont})}{D} \tag{2.7}$$

If, furthermore, $S_{cont} \ll F_{av} H(U)$, we obtain

$$Q \approx \frac{1}{\varepsilon\varepsilon_0 \rho\omega} \left(\frac{D}{F_{av}} \right)^2 \tag{2.8}$$

Consider now the quality factor for the device with strips (Fig.4). When $H(U) \ll F_{av}$ one can write

$$R \approx \frac{\rho_{av} \Delta}{D H(U)} \tag{2.9}$$

Δ being the gap between strips and ohmic contact. So, we obtain

$$Q \approx \frac{D^2}{F_{av} \Delta} \frac{1}{\varepsilon\varepsilon_0 \rho\omega} \tag{2.10}$$

Comparing (2.8) and (2.10) it is seen that using conductive strips one is able to improve the figure of merit by a factor of $\frac{F_{av}}{\Delta}$, which can be easily made to be about 100 for not too small (high-power) devices.

2.2 Varicaps using uniformly doped films

Devices with prescribed $C(U)$ characteristics can also be fabricated using films, which are uniform both in thickness and doping (see Fig.5). In that case, however, the substrate must be nonuniformely doped [13] (in x-direction). Substrate doping is increased along x coordinate within the active region of the varicap and outside that region the substrate is heavily p^+-doped. As shown in Fig.5 SCR region in the substrate diminished continuously with x, whereas the SCR region in the film is increased with x. As before, the space-charge region gradually fills the whole active volume of the device under increased reverse bias applied to the varactor. So, the effective area of the capacitor's plates is smoothly

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decreased. If substrate and film are made off the same material we can write for the capacitance-voltage characteristic an equation quite similar to (2.4):

$$C(U) = \varepsilon\varepsilon_0 \int_0^{H(U)} \frac{F(x)}{d(x,U)} dx \qquad (2.11)$$

but now

$$U + U_{bi} = \frac{q}{\varepsilon\varepsilon_0} \int_0^{d_1(x,U)} yN_d(x,y)dy + \frac{q}{\varepsilon\varepsilon_0} \int_{d_1(x,U)}^{d_2(x,U)} yN_a(x,y)dy \qquad (2.12)$$

supplemented by equation of electroneutrality for semiconductor

$$\int_0^{d_1(x,U)} N_d(x,y)dy = \int_{d_1(x,U)}^{d_2(x,U)} N_a(x,y)dy \qquad (2.13)$$

with obvious relationships (see fig.5)

$$H(U) = x, \quad \text{when} \quad d_1(x,U) = D \qquad (2.14)$$

and (in Eq.2.11)

$$d(x,U) = d_1(x,U) + d_2(x,U) \qquad (2.15)$$

In equations given above $d_1(x,U)$ and $d_2(x,U)$ are SCR thickness in the film and substrate, respectively, $N_a(x,y)$ is impurity distribution in the substrate, $N_d(x,y)$ is impurity distribution in the film.

The calculated $C(U)$ characteristics are presented in Fig.6 for varactors with uniformly doped silicon film (0.5 μm thick) with donor concentration 10^{16} cm^{-3} grown on the substrate having linearly increasing acceptor concentration (from 10^{15} to 10^{16} cm^{-3} over the active region of the device, as shown in Fig.6 (b)). To demonstrate the versatility of the technique we have calculated capacitance-voltage curves for three different shapes of the active region: two triangular and one rectangular as shown in the insert of Fig.6 (a).

2.3 Varactors saving chip area

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Since nowadays everyone in the field is concerned with *micro-* (and even *nano-*, not *milli-*, as depicted in Fig.6) electronics, it may be of interest to consider varicaps, which provide sufficiently large capacitance within a generally quite limited chip area available [5]. Our approach can easily be adapted for this important task also (cf. [14]). An example is shown in Fig.7 where the varactor is fabricated in the form of a periodic 3D structure from uniformly doped layer using anisotropic etching of silicon. Silicon microbumps with precalculated cross-section must be provided by Schottky contact (or p-n junction or MIS structure) over their whole surface (side face included). Basic principle is the same – electrically tuned electrode's area. The cross-section of the silicon pillars shown in Fig.8 was calculated for most important *linear* varicap.

2.5 Clino-varicaps

Now we would like to return to wedge-shaped films simply because the first experimental verification of our ideas has been accomplished (in 1994-1995) using exactly that (most difficult and inconvenient) way [15]. Device is fabricated from uniformly doped film grown homoepitaxally on the substrate with opposite conductivity type (Fig.9 (a)) or even insulating (semi-insulating), as the case may be (Fig.9 (b)). Etching can be used for the formation of the wedge-shaped active region. In fact, we simply dip slowly the semi-insulating GaAs substrate with MBE grown n-type epilayer into $H_2SO_4 - H_2O_2 - H_2O$ etching solution. If the composition of the etching bath and its temperature are held constant, then only dipping rate determines the inclination angle of the wedge, which can be easily controlled to within $\pm\ 0.1^0$. Then, the shape of the top Schottky contact can be calculated for almost *any* desired $C(U)$

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characteristic. Examples are presented in Fig.10 for $C/C_{\max} \sim (1-V/V_{\max})^n$ with n=1, 2, 3. Certainly, photolithography on the wedge –shaped samples is far from being trivial but, nonetheless, can be performed (painstakingly!), if inclination angle is small enough (and personal is sufficiently skilful and patient). A picture of a real device is shown in Fig.11(a) with measured $C(U)$ curve presented (not for the device shown, but, naturally, for the best from about dozen tested) in Fig.11(b). The (root-mean-square) deviation from *designed linear capacitance-voltage characteristic* was less than 5%, which certainly confirmed our expectations.

Now we can go to the **main topic** of the present work.

3. Intelligent semiconductor capacitance (capacitance transformer)

From a circuit designer's point of view any diode is no more than a non-linear resistor whereas a transistor is simply a voltage-controlled non-linear resistor – its output impedance is controlled by input signal. Quite similar to these trivial facts, an *intelligent*[2] semiconductor capacitor (SIC) is a device whose output capacitance is controlled by a signal applied to the input [16-19]. So, in contrast to varicap (or varactor), which usually has only two external leads (see, however, [20, 21]) SIC is a three- (or more)-terminal device. Due to this special feature we envisioned that application field of SICs is vastly expanded in comparison with

[2] We use this term only to emphasize that a device was born literally on the tip of the pen of the first author and has been materialized only some years after. This is in contrast to varicaps originated from p-n junction capacitance, which first have been measured on already existing diodes, and only then find their use in frequency tuners, frequency transducers, parametric amplifiers, etc.

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application field of traditional varicaps (in approximately the same ratio as application range of transistors exceeds that of diodes).

Intelligent semiconductor capacitors (capacitance transformers) can be used for amplification and frequency transformation and are highly superior to transistors as concerns the useful power delivered to the external load since temperature constraints are greatly reduced (capacitors are heated only in the inverse proportion to their Q-factor) and the so called electronic constraint, routed in breakdown voltage of any semiconductor junction[3] is almost *completely eliminated* in the SICs. Intelligent semiconductor capacitors fit nicely into existing integrated circuit technology. Moreover, capacitance transformers are highly preferential against usual inductive transformers from both technological and economic viewpoints and, we believe, could replace them at least in high frequency (and even microwave) range.

3.1 SIC operational principle explained

Let us consider a capacitance transformer (SIC) comprising a p-n junction with n-layer doped nonuniformely along x-coordinate (see Fig.12). On the top surface of this p-n junction a dielectric layer is grown having a metallic electrode thereon. Both n and p regions are provided with ohmic

[3] Exactly this is a reason that a maximum power delivered by any semiconductor device to the external circuit is inversely proportional to the square of operating frequency.

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contacts so that a reverse bias can be applied to the p-n junction. Let doping concentration in the active region of n-layer $N_i(x, y)$ (where $0 \le x \le x_{\max}$, $0 \le z \le F(x)$, and $y \le d$,) increases in some predetermined manner from $x_{\max}$ toward 0. Then, with increasing reverse bias the neutral (undepleted) region, $H(U)$, would shrink and effective area of SIC electrodes (between neutral region and metallic overlayer) would also decrease. Thus, we see that concurrently with usual drop of p-n junction depletion capacitance to which bias is applied, another capacitance changes – that between undepleted part of n-layer under dielectric and metal film. It is exactly this capacitance, which we call SIC (see Fig.12(a)). If $C_{sic}(t)$ is time-dependent capacitance of SIC, Q_{sic} is the charge on SIC electrodes, then voltage on SIC will be given by

$$V_{sic}(t) = \frac{Q_{sic}}{C_{sic}(t)} \qquad (3.1)$$

So, applying a voltage to the contacts of semiconductor junction we can control the voltage on the SIC. Evidently, the charge to the SIC can be supplied trough the load from external source (dc and/or ac). In that case the current and voltage on the load are controlled by input SIC signal, quite similar to transistor or electron tube. Note also that SIC can be fabricated from any varactor, if additional insulating layer is formed on its surface with metallic electrode on top.

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First of all, however, one *extremely important feature of newly proposed device should be emphasized*. The point is that SIC is inherently able to overcome a very fundamental constraint of each and every current semiconductor device, namely, the so-called "electronic constraint" on the maximum power deliverable to external circuit. The constraint mentioned stems directly from the fact that under the influence of applied bias (direct or reverse) the space-charge layer thickness is changed in the device. If, for example, we wish to extract the highest possible power from a bipolar transistor, then the voltage in the output (collector) circuit ought to be varied within the largest possible margins, i.e. from full depletion (never achievable in practice) to full neutrality (also never achievable). But saturated electron drift velocity (V_S) does not allow accomplishing the voltage variation instantaneously, and we conclude that a thickness of the collector is limited (at high frequencies, f) to the value of about $\frac{V_S}{f}$. If the collector is thicker, than additional ohmic losses are inevitable. In its turn, the maximum voltage applied to base-collector junction is limited by the breakdown voltage of that junction. It follows immediately that maximum power developed on the load is of the order of

$$P_{\max} \approx E_{bd}\left(\frac{V_S}{f}\right)^2 \frac{1}{R} \qquad (3.2)$$

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where E_{bd} is the breakdown electric field of the junction concerned and R is the load resistance. These considerations are *quite general and may be applied to any semiconductor device.*

*The **SIC** is free from this constraint* (at least, as output circuit is concerned) and its output power is determined only by Q-factor of the system. Thus, it allows to easily transformate the low-power low-frequency input signals into high-power high-frequency output. In that respect, we believe, the SIC *is second to none* in the field of semiconductor electronics. The output circuit of SIC-based frequency transducer is drived by alternating current of relatively low frequency, which is transformed into high-frequency signal in the same circuit.

As is shown in Fig.12(a) we have a low power high-frequency source in the input circuit of the device. In order to minimize the output/input cross-talk one can increase a thickness, H_d, of insulating layer and/or to put additional capacitor ($C_{||}$) in parallel to semiconductor junction (see fig.12 (b) depicting equivalent circuit of the device).

From theory of parametric amplifiers it is well known that amplifier is most effective when

$$mQ \approx 1 \qquad (3.3)$$

where m is the capacitance modulation coefficient and Q is the quality factor of the circuit containing capacitance being modulated. At first

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glance, it seems that an increase in insulator thickness (H_d) would inevitably result in substantial worsening of the modulation coefficient and, as a consequence, in poor device performance at high frequencies. Contrary to common sense expectations, we will show below that mQ product is, in fact, independent of insulator thickness for properly designed SIC.

To obtain simple analytical estimates let us consider Fig.13, which represents SIC device having a grid-like ohmic contact fabricated on n-type layer (period ***a***, metal stripe width $\mathbf{a_1}$) with an insulating layer (i-layer) on top. By the way, this i-layer can be fabricated separately and simply pressed onto main device body.

In this device the tuning range ($K=C_{max}/C_{min}$) is obviously reduced for thick i-layer. Let us calculate the C_{min}. In the literature [22] one can find the solution for analogous problem expressed through the elliptical functions, but the results obtained (or their approximations expressible through the elementary functions [23]), are not reproduced here, since application of these bulky formulae to the case at hand is too lengthy and, in fact, unnecessary. Our solution given below is much shorter and, at the same time, is sufficiently accurate for engineering estimates.

For $H_d>>a>>a_1$ (where H_d is the dielectric layer thickness, see Fig.13) the potential in the arbitrary z-plane cross section of the insulator

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is a sum of the grid potential (with a period a along x-coordinate) and potential of the top-most metallic electrode. It can be written as

$$\varphi = A\cos\left(\frac{x}{2\pi a}\right)\exp\left(-\frac{z}{2\pi a}\right)+\frac{\delta}{\varepsilon}(z-H_d) \qquad (3.4)$$

The first term in this expression describes the periodic potential originated from the grid, whereas the second term pertains to the potential induced by top electrode. By direct substitution on can confirm that (3.4) is a solution of the Laplace equation. In (3.4) δ is the surface charge density, ε is the dielectric constant of the insulating layer, and A is a constant. The parameters A and δ must be determined from boundary conditions. If a<<H_d the first term is vanishingly small and φ=0 for z=H_d. When z=0 (with $\cos\left(\frac{x}{2\pi a}\right)=-1$) we have for the potential of the contact

$$\varphi = A + H_d\frac{\delta}{\varepsilon} \qquad (3.5)$$

Periodic contact arrangement corresponds to an extremum of (3.4) at z=0 because contact's potential is a constant and any function variation near its extremum can be safely neglected. Differentiating (3.4) by z at z=0 (with $\cos\left(\frac{x}{2\pi a}\right)=-1$) and taking into account that potential near grid is a sum of grid potential = $\frac{1}{2}\frac{a}{a_1}\frac{\delta}{\varepsilon}$ and the top electrode potential =$\frac{1}{2}\frac{\delta}{\varepsilon}$ one obtains

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$$\frac{A}{2\pi a}+\frac{\delta}{\varepsilon}=\frac{1}{2}\frac{a}{a_1}\frac{\delta}{\varepsilon}+\frac{\delta}{2\varepsilon} \tag{3.6}$$

From this we have

$$A=\pi\left(\frac{a\delta}{a_1\varepsilon}+\frac{\delta}{2\varepsilon}-\frac{\delta}{\varepsilon}\right)=\pi a\frac{\delta}{\varepsilon}\left(\frac{a}{a_1}-1\right) \tag{3.7}$$

Since

$$C_{\min}\sim\frac{\delta}{\varphi}\sim\frac{\varepsilon}{H_d}\frac{1}{1+\frac{\pi a}{H_d}\left(\frac{a}{a_1}-1\right)} \tag{3.8}$$

and

$$C_{\max}\sim\frac{\varepsilon}{H_d} \tag{3.9}$$

the tuning range $K=C_{\max}/C_{\min}$ is given by

$$K=1+\frac{\pi a}{H_d}\left(\frac{a}{a_1}-1\right) \tag{3.10}$$

If, in parallel with p-n junction, a large capacitor ($C_{||}$) is switched in, we can write

$$K=\frac{2}{1+\frac{1}{1+\frac{\pi a}{H_d}\left(\frac{a}{a_1}-1\right)}} \tag{3.11}$$

For this case Q-factor and the maximum modulation coefficient m can be expressed as

$$Q\approx\frac{H_d d}{\varepsilon\rho\omega(a-a_1)};\qquad m_{\max}\approx\frac{K-1}{K+1}\approx\frac{\pi a}{2H_d}\left(\frac{a}{a_1}-1\right) \tag{3.12}$$

where ρ is the average resistivity of the active n-layer.

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From (3.12) one can see that a product m_{max} Q is indeed independent from H_d. Note also that in parallel-plate capacitor approximation one can write if $a_1 \gg H_d$

$$K = \frac{a}{a_1}; \qquad m_{\max} = \frac{\left(\frac{a}{a_1} - 1\right)}{\left(\frac{a}{a_1} + 1\right)}$$

If $C_{\|}$ is used one have

$$K = \frac{a}{2a_1}; \qquad m_{\max} = \frac{\left(\frac{a}{2a_1} - 1\right)}{\left(\frac{a}{2a_1} + 1\right)}$$

The device presented in Fig.13 allows (when $a \ll d$) to use n-layers for which the pinch-off voltage is larger than breakdown voltage and to enhance the Q -factor even further.

It seems that some specific example will be helpful at this point.

3.2 A worked example

Below an estimate of relevant parameters is given for the SIC to be used as a frequency converter from $f_{\min}$ = 1 GHz to $f_{\max}$ =5 GHz with 200 W peak power delivered (note, that if any of the existing varactors is used for the same purpose the power available will be at least *two orders of magnitude* lower).

Applied to the p-n junction is a signal with $f_{\max} - f_{\min}$ =4 GHz, whereas to SIC a signal with $f_{\min}$ =1 GHz is applied, and a tuned

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resonance circuit with a resonance frequency $f_{\max} + f_{\min}$ is used. An estimation of the SIC basic parameters proceeds then as follows:

1. Contact grid period must obey the obvious constraint

$$a < \frac{V_S}{f_{\max} + f_{\min}} = \frac{1\times10^5\, ms^{-1}}{6\times10^9\, s^{-1}} \approx 17\mu m \tag{3.13}$$

where V_s is the saturated electron drift velocity in Si (=1×10^5 ms^{-1}).

2. Let the insulating layer be fabricated from quartz (with a breakdown electric field $E \approx 10^9 Vm^{-1}$) and let a thickness of this layer to be about 100 μm. Then,

$$K = \frac{2}{1+\dfrac{1}{1+\dfrac{\pi a}{H_d}\left(\dfrac{a}{a_1}-1\right)}} \approx 1.4 m_{\max} \approx \frac{1+K}{1-K} \approx 0.2 \tag{3.14}$$

3. The horizontal dimension of n-base (a_x) can be chosen from the condition

$$a_x = \frac{\lambda}{20} = \frac{c}{20 f_{\max}\sqrt{\varepsilon}} \approx 1.5\ mm \tag{3.15}$$

the maximal capacitance being then

$$C_{\max} = \frac{2\varepsilon a_x^2}{H_d} \approx 1.5\times10^{-12}\ \text{F} \tag{3.16}$$

4. The doping level of n-base can be varied in a wide range. Let us choose the thickness of n-base to be 1 μm with doping level of n=1×10^{15} cm^{-3}.

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5. To find a maximum voltage to be applied to SIC and a minimum value of the capacitance ($C_{\parallel}$) to be switched in parallel with p-n junction, let us assume that a fraction of voltage, which drops on p-n junction, is 1 V. Then,

$$U_c = \frac{2PQ}{f_{\min}\sqrt{0.5C_{\max}}} \approx 1000 \text{ V} \qquad (3.17)$$

and for Q=10, P=200 W one finally obtains

$$C_{\parallel} = \frac{0.5C_{\max} \times U_c}{1\ V} = 7.5 \times 10^{-10} \text{ F} \qquad (3.18)$$

In this way, all relevant parameters of SIC-based frequency converter are now estimated. Fig.14 shows the calculated time dependence of the voltage on SIC (with parameters given above) for different modulation coefficients (in the figure, E is the amplitude of the lower frequency signal and m is the modulation coefficient).

3.3 Other circuit configurations with SICs

Here we would like to mention a couple of different configurations for circuit usage of SICs. Referring to Fig.15 (proposed by A. Maksutov) one can see that applying a reverse bias pulse to the p-n junction we can decrease the SIC (i.e., a capacitance between n-layer and top-most metal film), thus forcing the voltage on SIC to increase (see equation (3.1)). As a result the diode will be blocked and the SIC would discharge through the load resistance R_n. The maximum voltage on SIC is given by

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$$U_c \approx E\frac{C_{\max}}{C_{\min}} \qquad (3.19)$$

where E is the magnitude of the (constant) supply voltage, and $C_{\max}$ (C_{min}) is the maximum (minimum) of device capacitance.

Fig.16 shows capacitance transformer containing high constant voltage source (E) with a load resistor (R), connected to n-layer and aluminum metallization of SIC. The input signal $U = U_m \sin \Omega t + U_c$ is applied to p-n junction. Under the influence of comparatively small input signal the SIC will be modulated, being a part of high voltage circuit. The calculated time dependence of SIC voltage for that case is shown in Fig.17.

It goes without saying that SIC with metallic stripes placed over the active region (as shown in Fig.18) will have (greatly) enhanced Q-factor, and reasoning quite similar to that given at the end of subsection 2.1 leads to the conclusion that Q-factor of SIC is a factor of $\frac{H_d}{d}$ larger than Q-factor of corresponding varactor. As a consequence, SIC can be made fully operational for the frequencies up to *hundreds* GHz.

3.4 MIS-based SICs

Semiconductor intelligent capacitors can be also fabricated using metal-insulator-semiconductor (MIS) structures [24], as is shown, for example,

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in Figures 19-21. In case at hand the principle of SIC operation is closely related to well-known physics of normally "off" MIS transistors [3]. Consider, for example, Fig.19, which shows a typical p-MISFET with substrate back-surface provided by additional insulator layer coated by conductive (metallic) film. If positive bias is applied between the gate and anyone of the ohmic contacts, an inversion channel can be formed under the gate dielectric. As a result, the capacitance between ohmic contacts and bottom-most electrode (SIC!) will change. Obviously, high-resistivity semiconductor can be used as a bottom quasudielectric for frequencies

$$\omega \le \frac{1}{\varepsilon_0 \varepsilon \rho} \tag{3.20}$$

where ρ is the resistivity of the semi-insulating semiconductor.

Fig.20 shows yet another variant of MIS-based SIC with a semiconductor under gate dielectric (between source and drain) being nonuniformely doped along x-coordinate. Applying positive bias to the gate one should be able to produce an inversion channel under the gate which (due to nonuniform doping) will be also nonuniform thus allowing to smoothly vary the SIC between the ohmic contact and top-most electrode. Shaping the device active area allows one to vary SIC in a predetermined way. Evidently, source and drain contacts can be short-circuited but availability of *two* contacts is beneficial since transient

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processes of carrier dissipation are facilitated, which can be important for high-frequency applications. After all that have been said above, Fig.21 is, we believe, self-explaining, and we can go to the experimental part of our work.

4 Experimental

4.1 The first experience of SIC fabrication

In order to fabricate sufficiently flexible intelligent semiconductor capacitance one must be able to generate a laterally nonuniform impurity distribution under the gate in a controlled manner. In principle, focused ion beam implantation is uniquely suited for that purpose. The technique, however, was unavailable for us and we were forced to devise and use another approach.

One possible solution for the problem in question consists in using a two-layer masking technique, as shown in Fig.22. Impurity atoms enter through the narrow opening in the upper masking layer into second layer, in which the diffusion coefficient (D_1) is much larger than that in the semiconductor itself ($D_1 \gg D$). If silicon is used for device fabrication one can choose a polysilicon film as a second layer. Since $D_1 \gg D$ we can write for impurity distribution $N(x,t)$ in poly-Si

$$N(x,t) = \frac{Q}{\sqrt{\pi D_1 t}} \exp(-\frac{x^2}{4D_1 t}) \qquad (4.1)$$

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where Q is impurity surface concentration (atoms/cm^2) in the mask opening and x is the distance from the mask hole. In the single-crystal Si, then, impurity distribution is given by

$$N(x,z,t) = \frac{Q}{\sqrt{\pi D_1 t}} \exp(-\frac{x^2}{4D_1 t}) erfc\left(-\frac{z}{\sqrt{2Dt}}\right) \quad (4.2)$$

where z is the distance from c-Si/poly-Si interface. Practically, we have used even simpler method for generation of impurity distributions with lateral gradients. Combination of the methods just described allows one to produce almost any desired lateral impurity profile in a short time, which can be important if thin films are used for SIC fabrication.

We have fabricated the device shown schematically in Fig.23. The main body of the device consists of p-base (with an area 0.6-1.0 mm^2) having laterally nonuniform doping so that the acceptor concentration decreases from left to right. The length (L) of p-base along x-coordinate varied from 10 to 50 μm. Two ohmic contacts were fabricated: contact 1 to the active region and contact 2 for n$^+$-substrate. Gate oxide thickness was 0.2 μm. It was assumed that by increasing the reverse bias applied to p-n junction we could shrink in a controlled fashion the neutral region in the p-base along x-coordinate. Then, simultaneously with usual decrease of p-n junction depletion

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capacitance, we should observe a corresponding variation in SIC (measured between the gate contact and contact 1).

For device fabrication six silicon wafers were used (n-type, heavily Sb-doped to a concentration of electrons 5×10^{19} cm^{-3} with 12 μm - thick epitaxial layer on top doped to 10^{15} cm^{-3}, also n-type). In general, 12 different nonuniform p-type doping distributions along x-coordinate have been realized and tested in our work.

In order to obtain a nonuniform distribution of acceptor concentration along x-coordinate we have implemented the following approach. We perform a diffusion of acceptor impurity through the system of stripe openings in the masking oxide with pre-calculated variable widths. In this way, we were able to achieve almost linear variation of acceptor concentration in p-base in lateral direction. The basic idea of our trick is explained in Fig.24. Acceptor impurity is introduced into a semiconductor through an array of variable-width openings in the masking layer (width $H_0(x)$, inter-window spacing being fixed at H-const) followed by usual thermal annealing. Initially the impurity concentration in semiconductor under the mask is zero whereas in the windows it is determined by the time of drive-in diffusion or ion dose during implantation. For annealing times $t\approx H^2/D_a$ (D_a is impurity diffusion coefficient) acceptor atoms will penetrate under the masked regions due to lateral diffusion from neighboring

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windows. For the average ion dose D(x) in the section of the device near the specific x-coordinate with opening width $H_0(x)$ ($H_{min}<H_0(x)<H_{max}$) we can write $D(x)\approx P(x)D_0$, where D_0 is implant dose and

$$P(x) = \frac{H_0(x)}{H_0(x) + H} \tag{4.3}$$

$H_0(x)$ being the x-dependent width of the window, the function P(x) may be called the local mask transparency, because it is simply equal to the ratio of the open area to the sum of open and masked areas in the vicinity of a specific x-coordinate. Obviously, by varying the local mask transparency one should be able to create almost any desirable lateral impurity profile.

The final distribution of acceptor impurity in the base $N(\xi,x)$ can be easily estimated from a simple one-dimensional diffusion expression

$$N(\xi, x) \approx P(x)D_0(\pi D_a t)^{-\frac{1}{2}} \exp(-\xi^2 / 4D_a t) \tag{4.4}$$

where ξ is a depth under the surface. Fig 24 illustrates the resulting impurity profile for the mask with five openings having linearly decreasing (from H_0 to $0.2H_0$) window's width and fixed inter-window spacing ($H=H_0$). As can be seen from Fig.24 the time required to obtain a smooth impurity profile is about $H^2/0.25D_a$.Thus, using a

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standard diffusion through the system of variable-width openings in the masking layer we successfully solved the fabrication problem of controlled laterally nonuniform impurity distribution in semiconductor wafer.

In our experiments we used the boron doses (E=100keV) from 1×10^{12} to 3×10^{12} ions per cm^2 , annealing times have been varied from 14 to 30 hours and maximum (minimum) window widths used were 7μm (2.8 μm). Using this approach and the mask shown in Fig.25 we were able to fabricate a p-base, in which the boron concentration increases almost linearly toward the ohmic contact (contact number 1 in Fig. 23) from beneath the gate.

The pre-calculated value of the punch-through reverse voltage (U_p) for p-base in our devices have been expected to be less than 5V in all cases:

$$U_p = \max\left\{\frac{q}{\varepsilon_0\varepsilon}\int_0^d N_i(x,y,z)zdz\right\} < 5V \qquad (4.5)$$

We expected also that applying higher reverse bias ($U>U_p$) to the p-n junction we can force the space-charge layer to fill the whole body of p-base region and then the minimal value of SIC should be about 4-6 pF (depending on the specific device geometry). Both our expectations fail completely! Experimental C-U measurements indicate that full depletion of p-base is *never achieved for any reverse*

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bias. Contrary to our expectations a certain fraction (1/3-1/5) of the p-base material remains undepleted even at highest reverse bias used, see Fig.26. The ratio C_{min}/C_{max} was measured to be greater than 1/5, whereas the expected magnitude of this ratio should be less than 1/30. Moreover, the minimum value of SIC was practically independent of the gate voltage.

4.1 Explanation of measured results and refinement of device structure

For the fabrication of varactors and SICs with a large tuning range (C_{min}/C_{max}) two questions naturally arise in view of experimental results outlined in the proceeding paragraph:

1. Why full depletion of mobile charge carriers in a p-base region of a device is not achieved?
2. What have to be done in order to obtain the necessary full depletion?

To answer the first question a 2D simulation of our device was undertaken. Within standard drift-diffusion model [25] the following problem has been formulated and solved (see Fig.27):

$$\nabla^2\varphi = -\frac{q}{\varepsilon_0\varepsilon}(N_d - N_a + p - n) \tag{4.6}$$

$$J_n = -q\mu_n\nabla\varphi + q\nabla D_n n \tag{4.7}$$

$$J_p = -q\mu_p\nabla\varphi - q\nabla D_p p \tag{4.8}$$

$$\frac{dn}{dt} = 0 = -U + \frac{1}{q}\nabla J_n \tag{4.9}$$

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$$\frac{dp}{dt} = 0 = -U + \frac{1}{q}\nabla J_p \tag{4.10}$$

$$U = \frac{np - n_i^2}{\tau_n(p + n_i) + \tau_p(n + n_i)} \tag{4.11}$$

We used the following boundary conditions:

on the first upper ohmic contact (cf. Fig.27)

$$\varphi = \varphi_1;\ p = p_1;\ n = n_1;\ pn = n_i^2;\ n - p = N_d - N_a; \tag{4.12}$$

on the second ohmic contact, i.e. at the bottom and right-hand boundary of simulation domain (cf. Fig.27)

$$\varphi = 0;\ pn = n_i^2;\ p = p_1 \exp(-\frac{q\varphi_s}{kT});\ n = n_1 \exp(\frac{q\varphi_s}{kT}) \tag{4.13}$$

at the semiconductor-insulator interface the normal component of electron and hole current density is identically zero (cf. Fig.27), hence

$$J_{p_y} = 0;\ J_{n_y} = 0;\ \frac{d\varphi}{dy} = const = 0 \tag{4.14}$$

at the left-hand boundary due to symmetry

$$\frac{d\varphi}{dx} = \frac{dn}{dx} = \frac{dp}{dx} = 0 \tag{4.15}$$

In the expressions above the usual symbols have been used: φ is the potential, $J_n(J_p)$ is electron (hole) current density, $\mu_n(\mu_p)$ is electron (hole) mobility, $D_n(D_p)$ is electron (hole) diffusion coefficient, p(n) is hole(electron) concentration, q is an elementary charge, N_d-N_a is net doping concentration, ε is dielectric constant of Si, φ_s is a built-in barrier potential, n_i is intrinsic carrier concentration and $\tau_n(\tau_p)$ is

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electron (hole) lifetime (relaxation time). We used empirical relations $\mu_{n,p}=F(E, N_d-N_a)$ [25] where E is electric field and Einstein relation

$$\frac{\mu_{n,p}kT}{q} = D_{n,p} \tag{4.16}$$

in our calculations.

Fig.27 illustrates the solution obtained on a grid with equal space steps along x and y axes (5.0×10^{-8} m), $n_i=1.5\times10^{10}$ cm^{-3}, for p-base with doping concentration of 2×10^{15} cm^{-3}, upper contact width 0.5μm, $\varphi_s=0.8$V, and $\tau_n=\tau_p=10^{-8}$ s. Equipotential lines in Fig.27 correspond to the applied voltage of 8 V ($U=\varphi_1-\varphi_2= - 8$ V). Note that isopotential line for $\varphi= -7.9$ V approximately defines the boundary of the neutral region beyond which the potential changes insignificantly. It is clearly seen from Fig.27 that near the SiO_2/Si interface a neutral layer exists even for the reverse bias (U) twice as large as a punch-through voltage (U_p). An important conclusion can be drawn from this observation: the absence of the full depletion in p-base is not caused by faulty technological route. The true reason is that the lowest bias required for the full depletion of the SiO_2/Si interface is much larger than U_p. By extensive numerical work (using simply a trail-and error method) it was found that insertion of a thin n- or i-layer under the SiO_2 film rectifies the situation and allows to achieve full depletion for reverse biases $U\geq U_p$. This is illustrated by Fig.28 where equipotential lines are

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drawn for exactly the same conditions as in Fig.27, the only difference being that a layer of i-Si with $n \approx 2\times10^{10}$ cm^{-3} and a thickness of 5×10^{-8}m was inserted beneath the SiO_2.

To explain our finding in general terms let us consider Fig.29 where a semiconductor device is shown consisting of region (1) (which is chosen to be p-type) with a first ohmic contact (2) fabricated on the one part of the upper surface of the said region while on the remaining part of the surface an insulating layer (3) is formed with conductive contact (4) on it. On the bottom and (for simplicity) right-hand side of region (1) the Schottky contact (5) is fabricated with an ohmic contact (6) attached to it. To simplify the discussion it will be assumed that $N_i(x,y)=N_a-N_d=const$.

For the constant normal component of the electric field at semiconductor-insulator interface (E_y=const) which corresponds to the application of constant voltage (including zero) between ohmic contact (2) and gate contact (4), the Poisson equation near the interface

$$\frac{dE_x}{dx}+\frac{dE_y}{dy}=\frac{q}{\varepsilon_0\varepsilon}\left[p+n-N_i(x,y)\right] \qquad (4.17)$$

is simplified, and takes the form

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$$\frac{dE_x}{dx} = \frac{q}{\varepsilon_0 \varepsilon}\left[p + n - N_i(x,y)\right] \tag{4.18}$$

Since $E_x = -\frac{d\varphi}{dx}$ and for the fully depleted p-region (1) we have n,p<<N_i(x,y), one obtains from (4.18) at the interface with an isolating layer

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_0 \varepsilon} N_i \tag{4.19}$$

for $y = d$ and $0 \le x \le L$, where φ is the potential and L is the extension of active p-region under the insulator in x-direction. Solving this equation under conditions of $\varphi(0,d) = 0$ and $\frac{d\varphi}{dx} = 0$ at $x = d$, we obtain

$$\varphi(x,d) = \frac{q}{\varepsilon_0 \varepsilon}\int_0^x N_i(h,d)hdh; \quad \varphi(L,d) = \frac{q}{\varepsilon_0 \varepsilon}\int_0^L N_i(h,d)hdh; \tag{4.20}$$

Here, $\varphi(L,d)$ is a minimal voltage drop between contacts (2) and (6) that guarantees the full surface depletion of mobile charge carriers in p-region at the interface with isolating layer. $\varphi(L,d)$ includes a built-in potential (φ_s), i.e. a potential drop in p-region in the absence of any external bias.

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If $L >> d$ and, under depletion conditions, we obviously have that $N_i(x,y) >> n, p$, one can safely assume that potential is changing along y-coordinate much faster than along x-coordinate and, therefore, the Poisson equation (since $E_x = -\frac{d\varphi}{dx}$ and $E_y = -\frac{d\varphi}{dy}$) can be written as

$$\frac{d^2\varphi}{dy^2} = \frac{q}{\varepsilon_0 \varepsilon} N_i(x,y) \tag{4.21}$$

with boundary conditions

$$\varphi(x,0) = 0; \quad \frac{d\varphi(x,y)}{dy} = 0 \tag{4.22}$$

The solution of (4.21) under conditions (4.22) can be found immediately

$$\varphi_1(x,y) = \frac{q}{\varepsilon_0 \varepsilon} \int_0^y N_i(h,d)\,hdh; \quad \varphi_1(x,d) = \frac{q}{\varepsilon_0 \varepsilon} \int_0^d N_i(h,d)\,hdh; \tag{4.23}$$

Here, $\varphi_1(x,d)$ is a minimal voltage between contacts (2) and (6) in Fig.29 when a depletion of p-region occurs in the bulk for x-section with $0 \le y \le d$. Obviously, $\varphi_1(x,d)$ includes a built-in potential φ_s at the

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semiconductor-insulator interface. Note that $\max\{\varphi_1(x,d)\} \equiv U_p$ - a punch-through reverse voltage for the full depletion of the bulk of p-region in x-section of the device.

Let U_i be the breakdown voltage of the p-base material. Then for $U_p < U_i$ and $\varphi(L,d) < U_i$ the bias to be applied between contacts (2) and (6) in Fig.29 for the full depletion (bulk and interface) of the p-region (1) must fulfill the following requirements

$$U > U_p \quad \text{and U} \geq \varphi(L,d) \tag{4.24}$$

Under these conditions the space-charge layer will extend to the whole volume of p-base region (1) in Fig.29. If

$$U_p < U_i \text{ and } \varphi(L,d) > U_i \tag{4.25}$$

then for the bias $\varphi(L,d) \geq U \geq U_i$ the space charge region of a reverse – biased p-n junction fills the whole p-base except a thin layer underneath ohmic contact and a part of insulating layer which remains undepleted (see Fig.23 and Fig.29).

Now, if we provide a thin layer under the insulating film and this layer:

1) will have an opposite conductivity type with respect to the main body (1) of the device, and

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2) a thickness of the layer will be only a fraction of the screening length,

then, obviously, the surface of this layer in contact with an insulator will be depleted of mobile charge carriers from the very beginning.

This simple fact explains the results of more elaborate 2D-simulations, as well as the results of C-U measurements presented in fig.30. Shown in this figure are experimental measurements of SIC (between ohmic contact (2) to the active region (1) and gate metallization (4)) for devices *without* (curve A) and *with* (curve B) n-type layer beneath SiO_2. The n-type layer under the gate oxide was fabricated by phosphorus ion implantation (energy 70keV, dose $1.5\times10^{11}cm^{-2}$) before thermal oxidation. With n-layer in place, the calculated value of SIC is in satisfying accordance with measured results.

5. Conlcusion

Hopefully, in the present article a simple fact has been amply demonstrated: there is a plenty of room in the field of classical semiconductor science and technology, if one is willing to improve existing and to create some new devices without invoking so fashionable recently quantum effects. In any case, it seems useful from time to time to have a fresh look at old things.

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Figure captions

Fig. 1 Non parallel plate semiconductor capacitance with electrically tuned electrode's area realized on a wedge-shaped sample. $L = L(U)$ and $d = d(U)$ designate effective length of the electrode and space-charge region width for reverse bias U, respectively.

Fig. 2 Planar varactor with electrically modulated electrode's area due to nonuniformely doped active region.

Fig.3 Calculated shape of the active region for linear varicap.

Fig.4 Varactor with highly conductive stripes on the surface of the active region, which are used to provide an enhanced quality factor of the device.

Fig.5 Varicap with electrically tuned electrode's area using constant thickness uniformly doped film and non-uniformly doped substrate.

Fig.6 (a) The shape of the active region (insert) and corresponding C(U) characteristics for the varactor with uniformly doped film (N_d=10^{16} cm^{-3}, D=0.5 μm, x_{max}=1 mm, U_{max}=20.2 V, U_{min} =3.1 V, C_{max}=105 pF). (b) shows impurity distribution in the substrate within the active region of the device presented in Fig.5.

Fig.7 The general view of chip – area – saving varicap, which can be fabricated by anisotropic etching of n-type Si film on p-type Si substrate.

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Fig.8 Calculated cross-section shape of the silicon bumps shown in Fig.7 for linear varicap (a/b=10, $N_d=10^{15}$ cm^{-3}, U_{max}=100V, substrate is degenerately doped p-type).

Fig.9 Clino-varicap fabricated on the wedge - etched n-type epilayer grown on heavily p-doped (a) or semi-insulating (b) substrate.

Fig.10 The shape of the active region for various $C(U)$ characteristics of clino-varicaps with sufficiently small inclination angle (when sinα~tgα~α)(a) and corresponding capacitance-voltage curves (b). $F_1(x)$ for $C/C_{\max} \sim 1-V/V_{\max}$, $F_2(x)$ for $C/C_{\max} \sim (1-V/V_{\max})^2$, $F_3(x)$ for $C/C_{\max} \sim (1-V/V_{\max})^3$.

Fig.11 Photomicrograph of a real device fabricated on wedge-shaped n-type ($n\sim10^{15}cm^{-3}$) GaAs film grown by MBE on semi-insulating GaAs(100) substrate (a), and best measured (f=0,5 kHz) $C(U)$ characteristic (b).

Fig.12 General outline of semiconductor intelligent capacitance (a) and its simplest equivalent circuit (b).

Fig.13 Cross-section of the SIC with grid-like ohmic contact to partitioned n-type active layer (as used for estimation of mQ product).

Fig.14 Time dependence of the voltage on SIC for two modulation coefficients (all other parameters of the frequency converter circuit are given in the text).

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Fig.15 Capacitance transformer with DC voltage supply and a diode. General outline (a) and equivalent circuit (b).

Fig.16 SIC with high constant voltage supply .

Fig.17 SIC voltage for the device shown in Fig.16 for different values of capacitance modulation coefficient. Inserts show an equivalent circuit (left) and equations used for calculation of the curves (right).

Fig.18 SIC with metallic (conductive) stripes over the active region.

Fig.19 Double-gated MISFET-based SIC.

Fig.20 MIS-based SIC with nonuniformely doped channel and multilayer gate.

Fig.21 Semiconductor intelligent capacitance using double-gated MISFET with nonuniformely doped channel.

Fig.22 Two-layer masking technique for producing laterally controlled impurity distributions in the active volume of the device.

Fig.23 Schematic representation of experimental device.

Fig.24 Diffusion mask configuration (a), and impurity profiles under the mask for different annealing times (b).

Fig.25 Fragment of the actual mask used for the fabrication of laterally nonuniform impurity distributions in a p-base of the device.

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Fig.26 Typical results of capacitance-voltage measurements.

Fig.27 Equipotential lines in p-base for $U=2U_p$.

Fig. 28 Equipotential lines in p-base with i-layer inserted beneath the SiO_2 film (all other parameters being identical to that of Fig.27).

Fig. 29 Illustrates why full depletion is impossible for device with a structure shown in Fig.23 (see text).

Fig.30 A comparison of the capacitance-voltage curves measured on SIC without n-layer under the gate (A), and with n-layer in place (B).

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Fig.1 Ioffe V M "New varactors…"

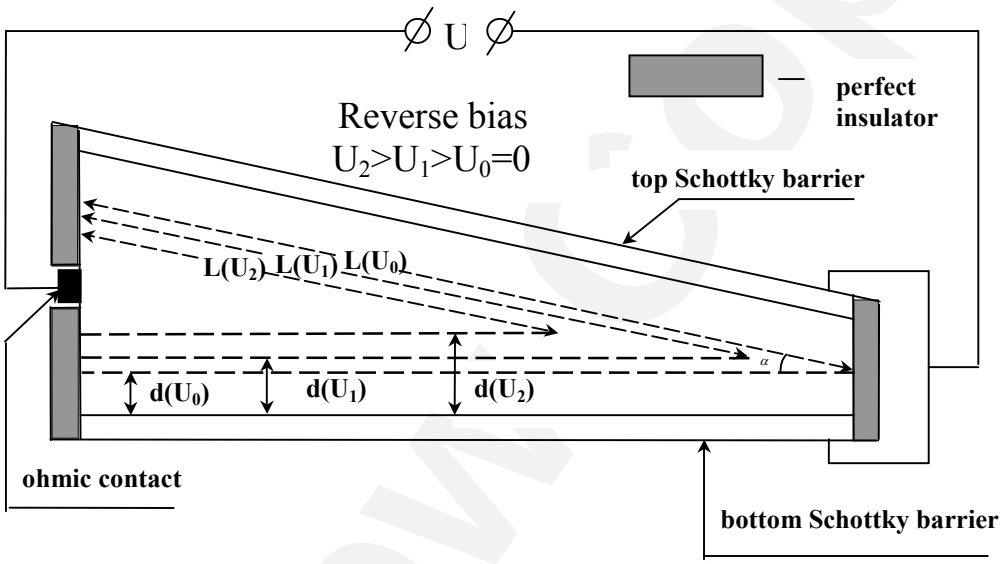

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Fig.2 Ioffe V M "New varactors……"

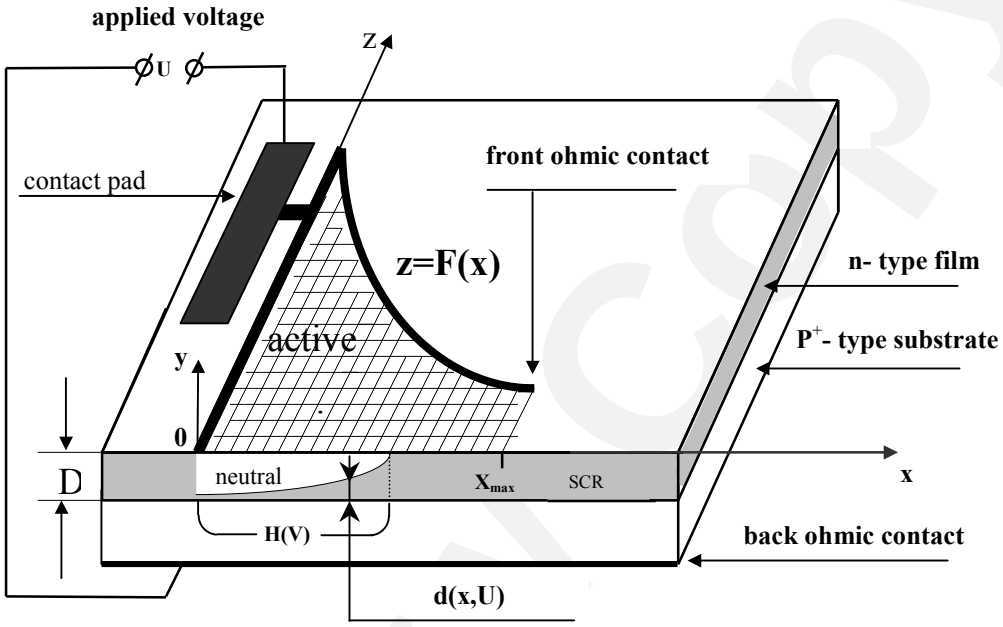

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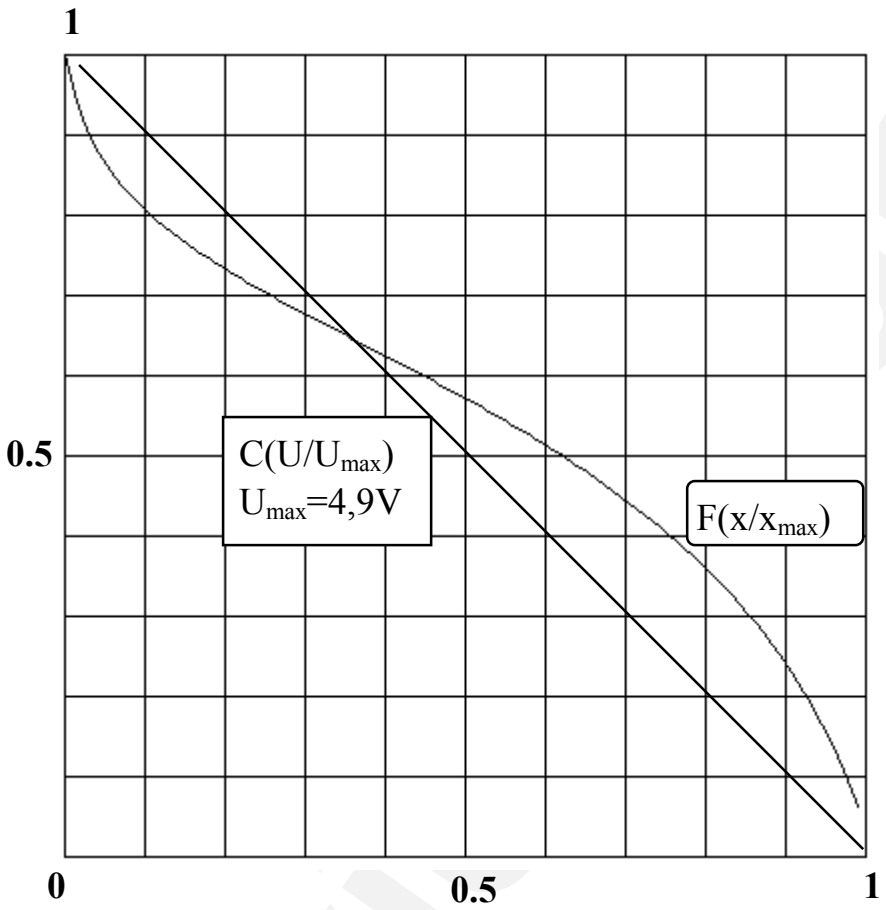
Fig.3 Ioffe V M "New varactors……"



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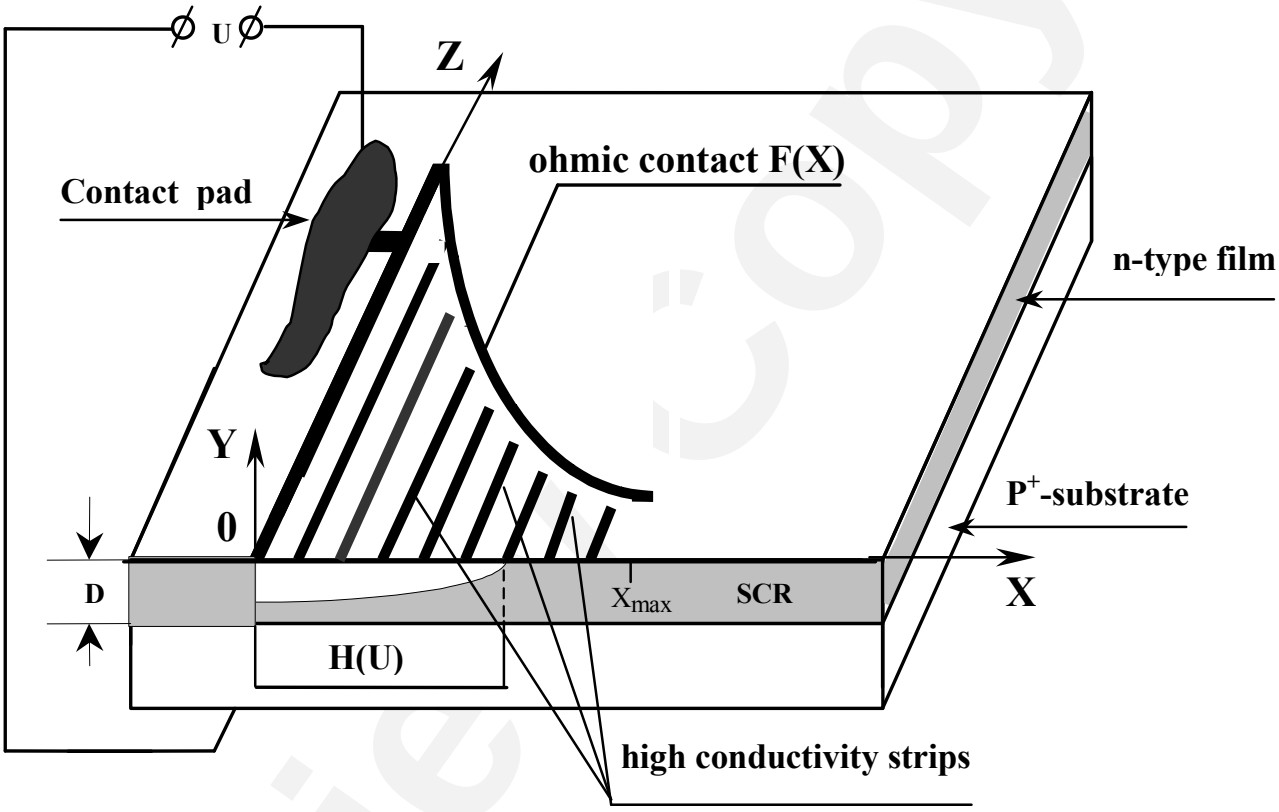

Fig.4 Ioffe V M "New varactors……"

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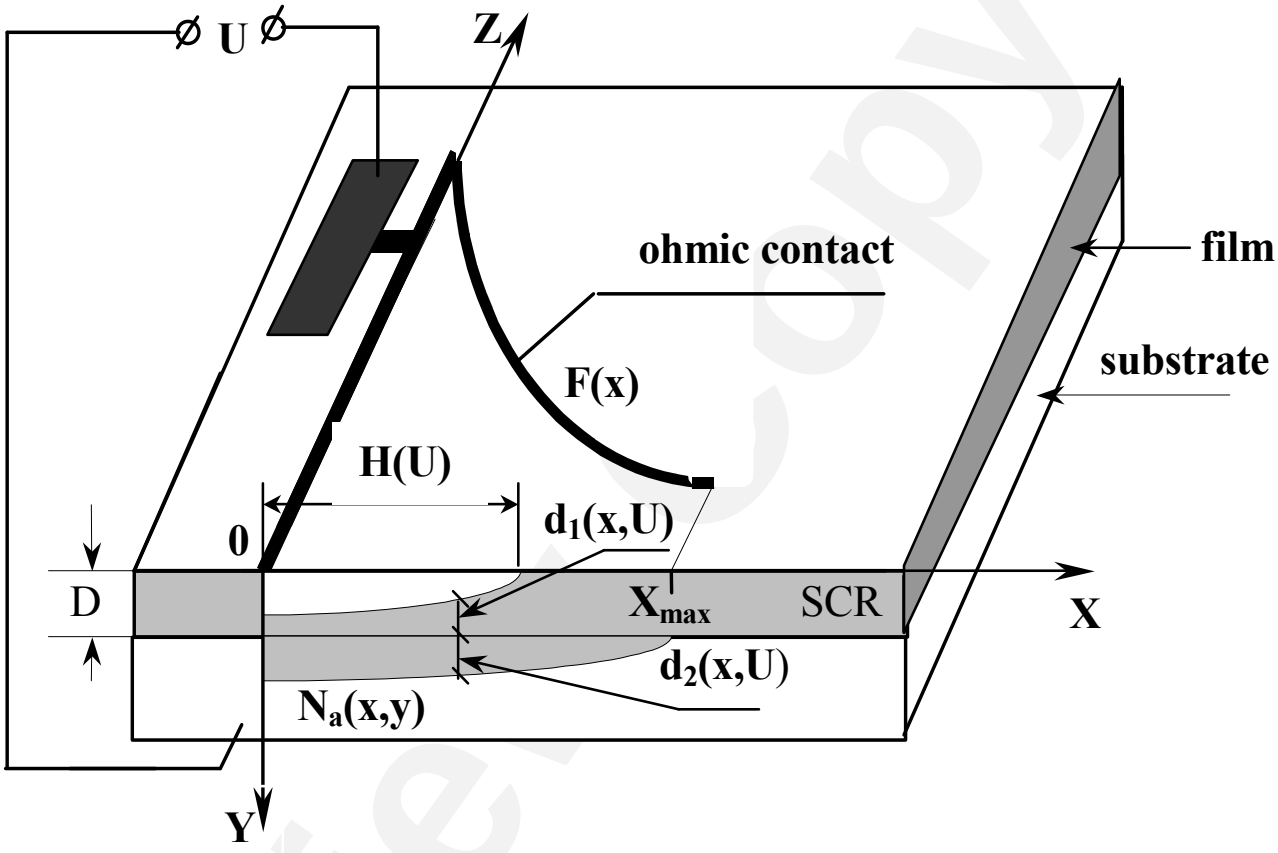

Fig.5 Ioffe V M "New varactors……"

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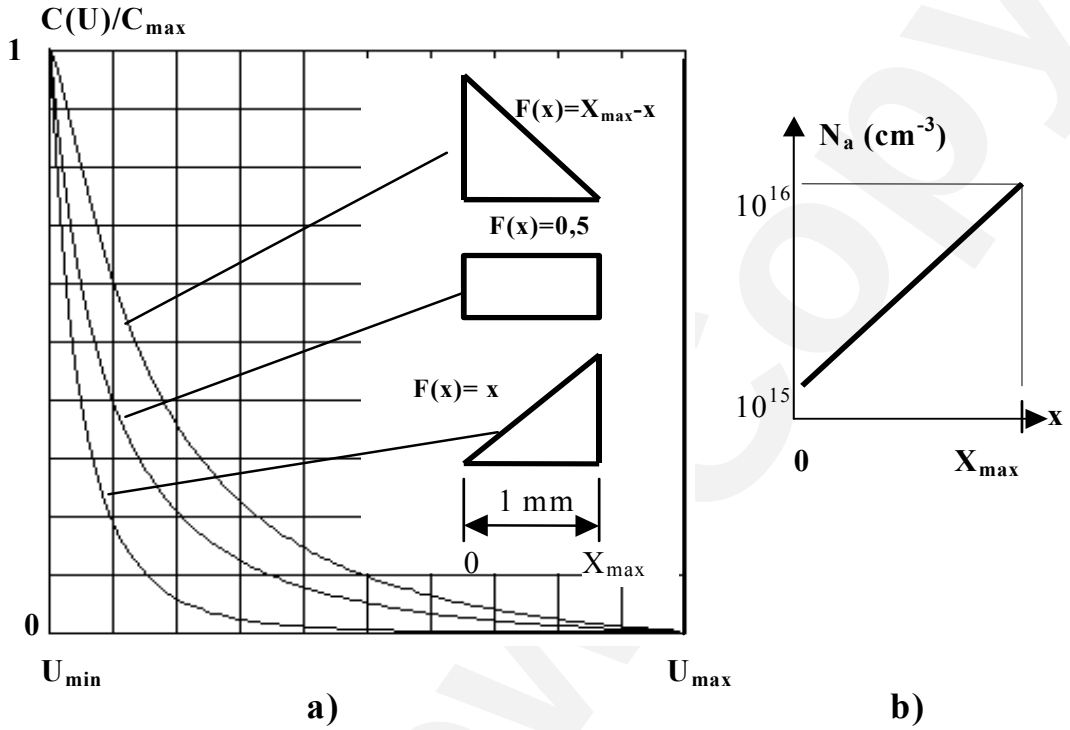

Fig.6 Ioffe V M "New varactors……"

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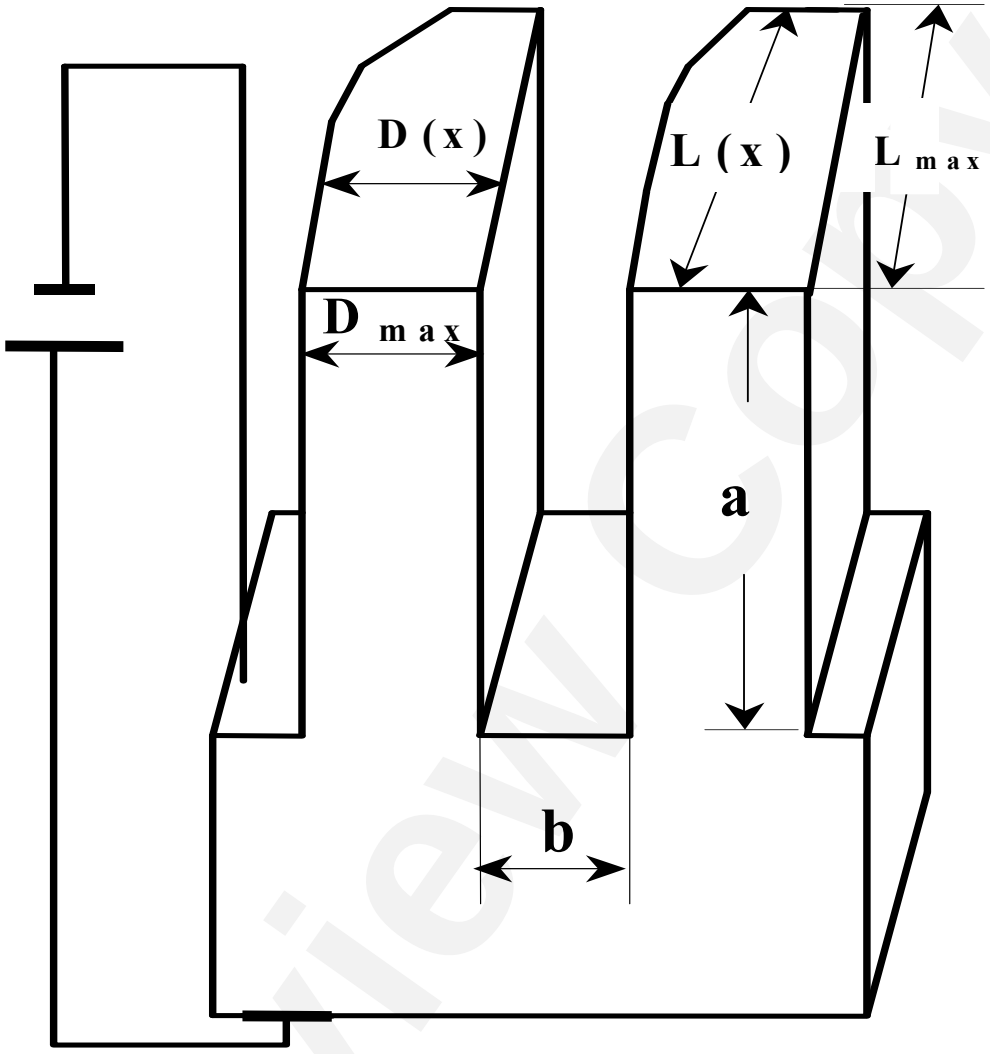
Fig.7 Ioffe V M "New varactors……"



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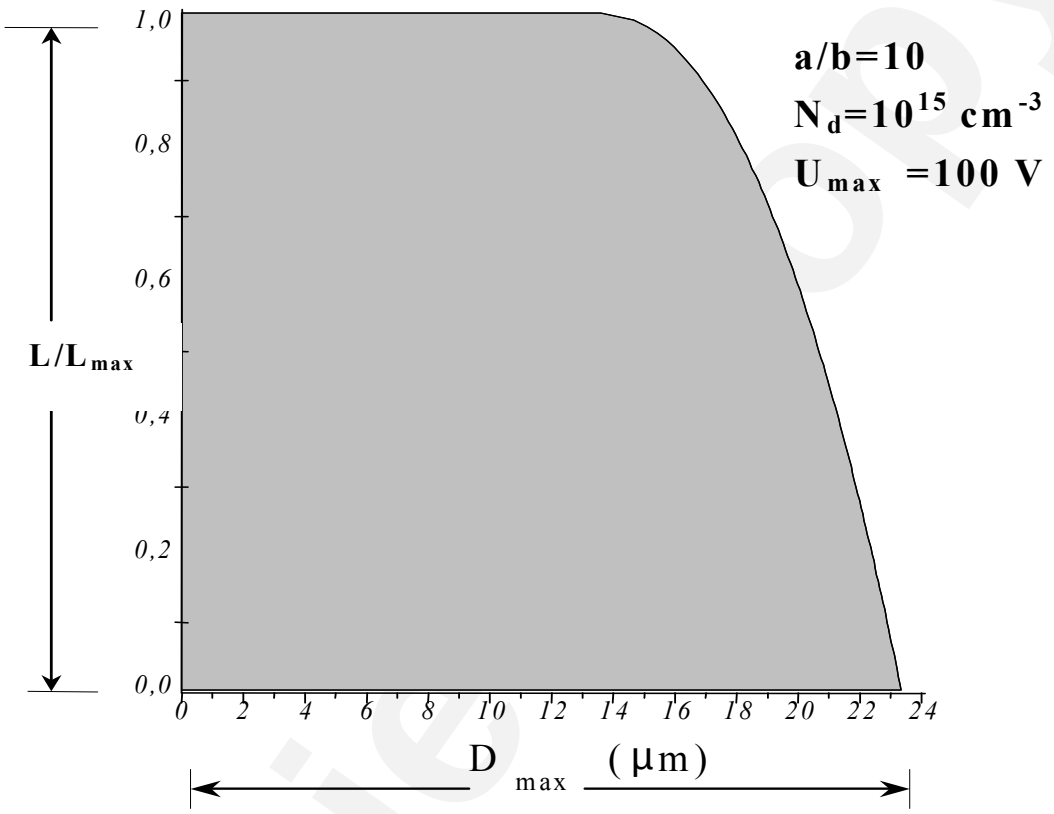

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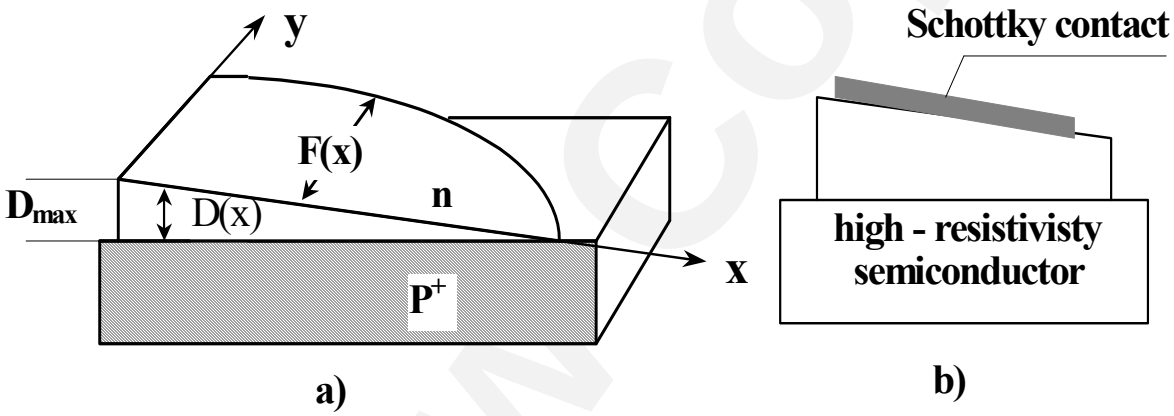

Fig.9 Ioffe V M "New varactors……"

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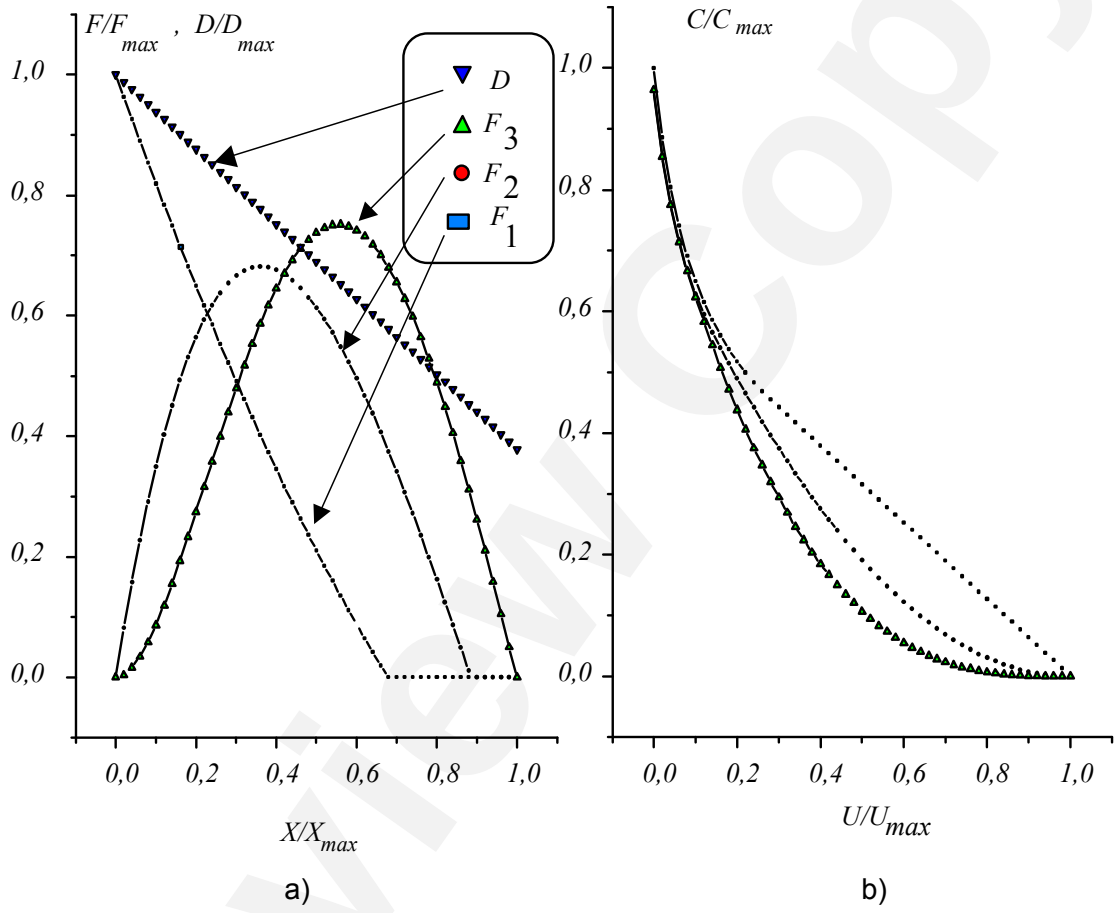
Fig.10 Ioffe V M "New varactors……"



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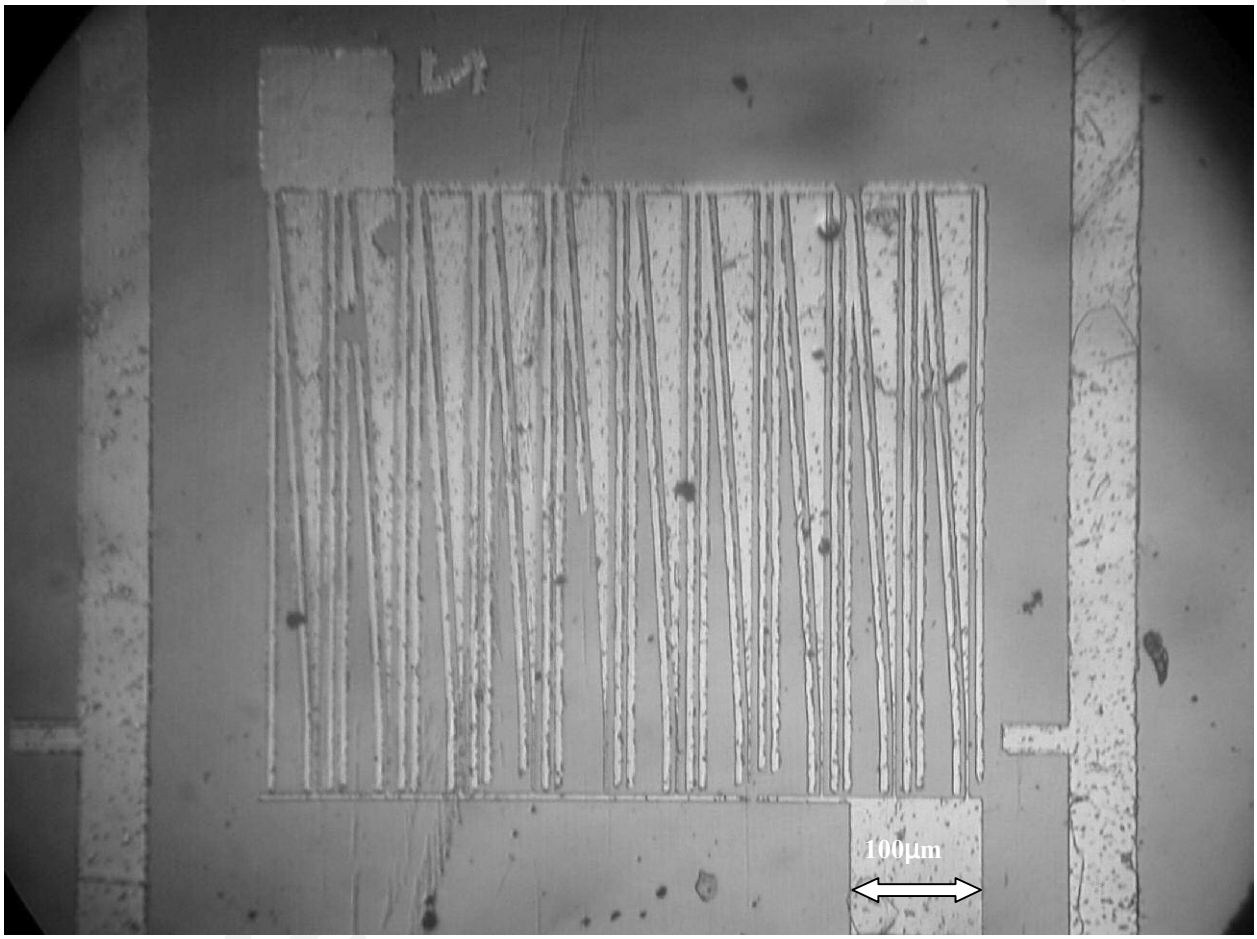
Fig,11(a) Ioffe V M "New varactors……"



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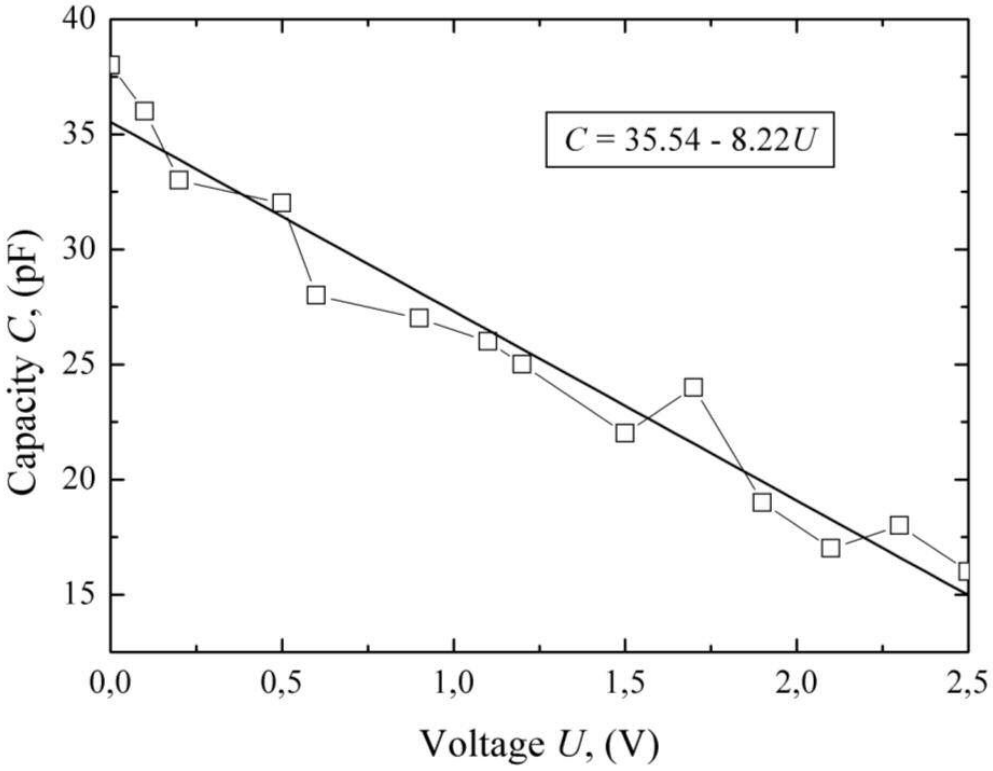

Fig.11(b) Ioffe V M "New varactors……"

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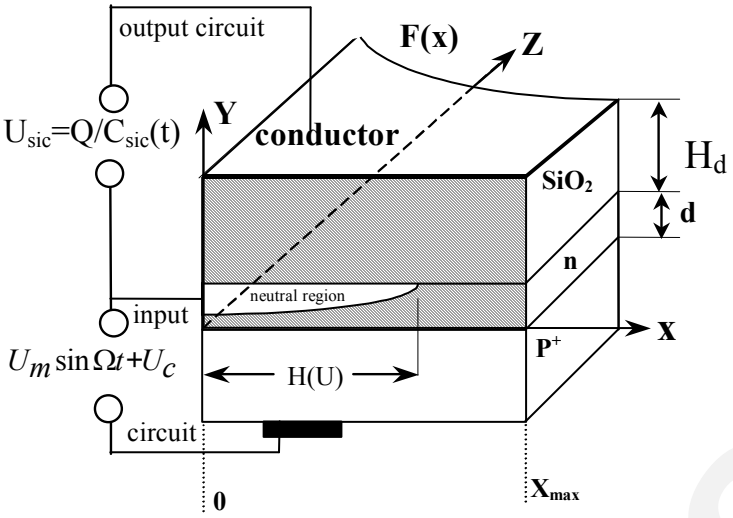
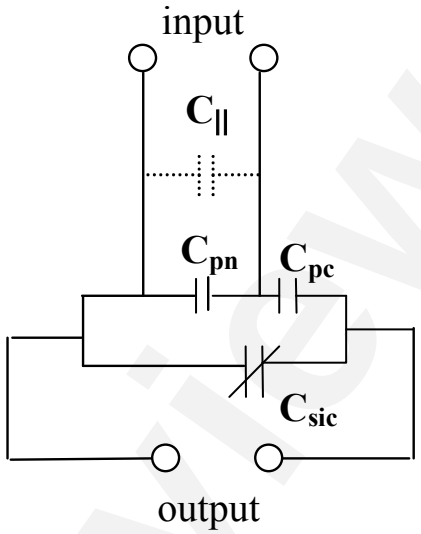


a)



b)

Fig.12(a,b) Ioffe V M "New varactors……"

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Fig.13 Ioffe V M "New varactors……"

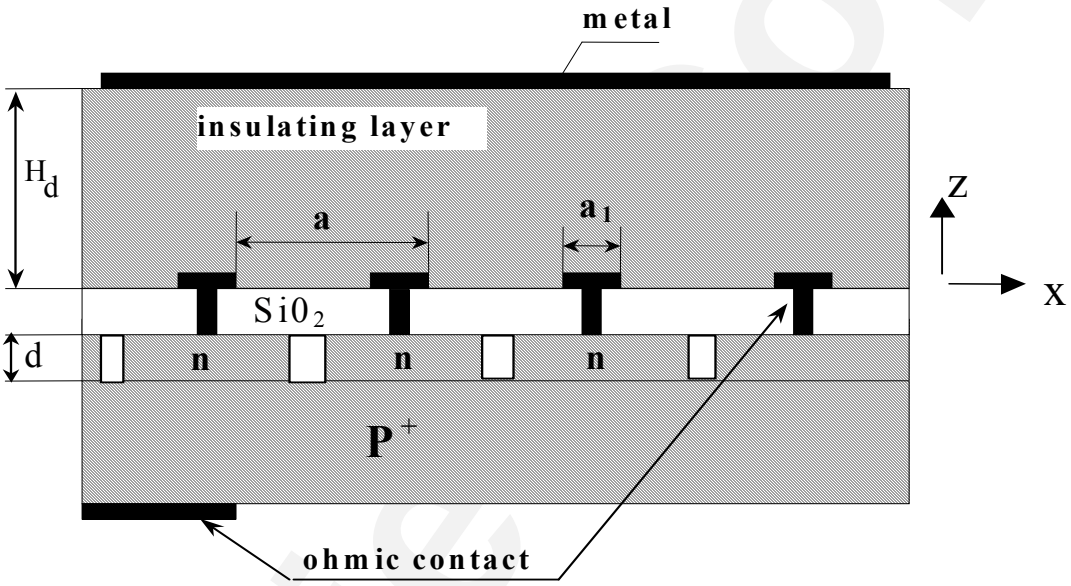

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Fig.14 Ioffe V M "New varactors……"

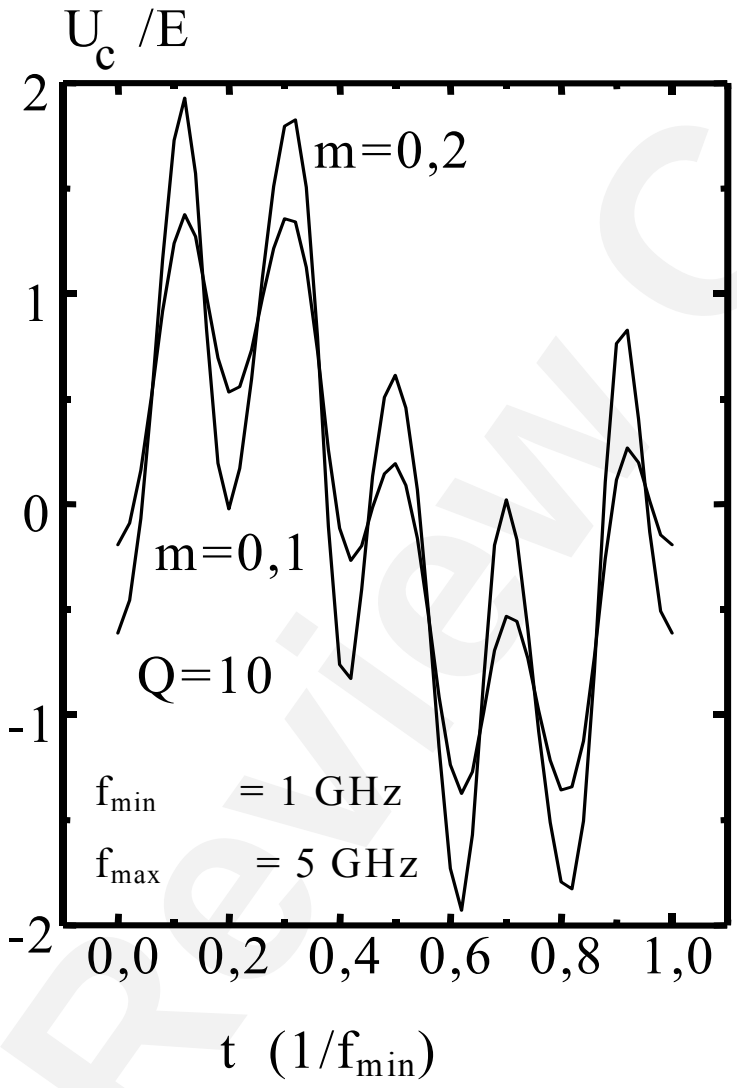

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Fig.15(a,b) Ioffe V M "New varactors……"

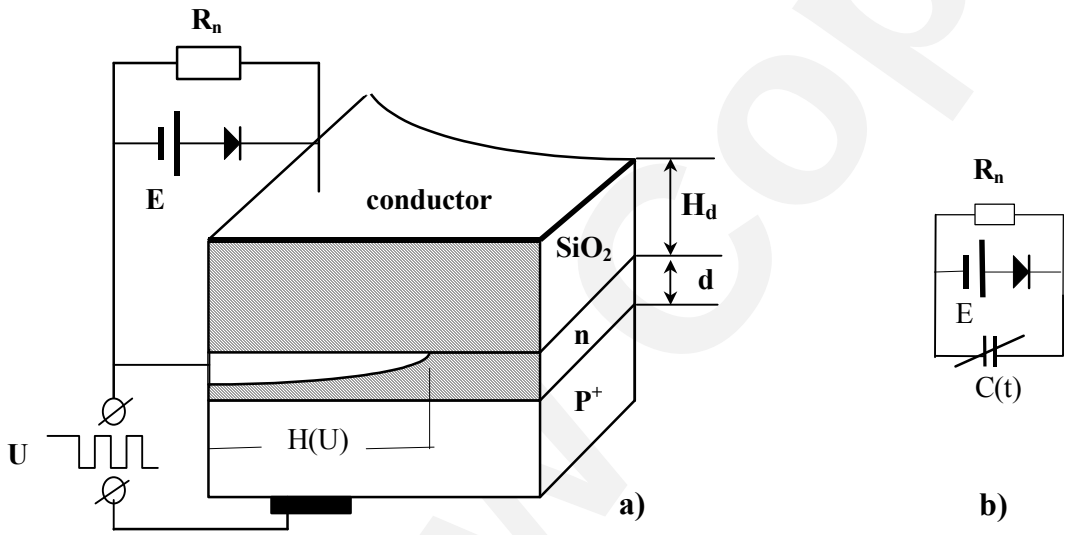

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Fig.16 Ioffe V M "New varactors……"

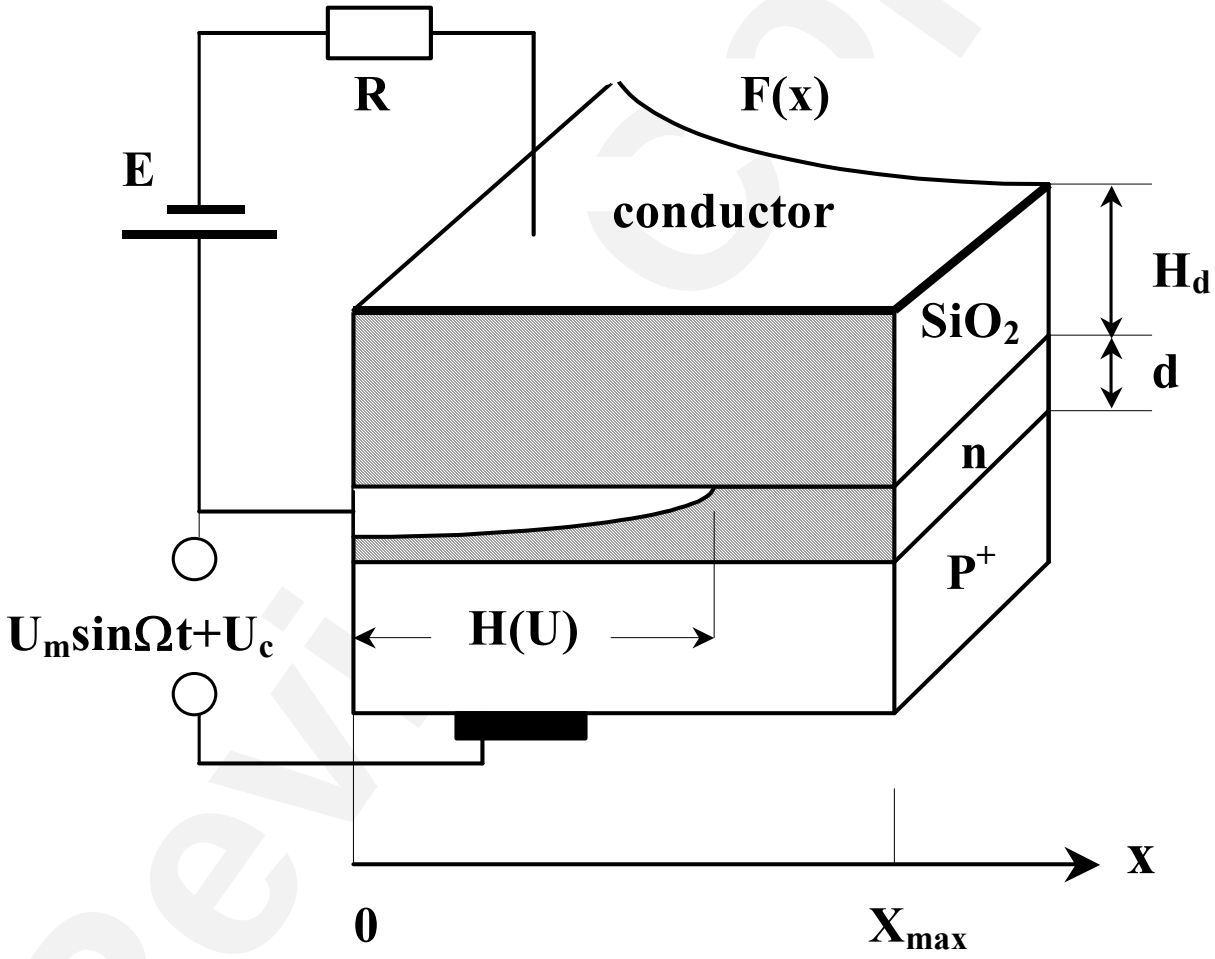

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Fig.17 Ioffe V M "New varactors……"

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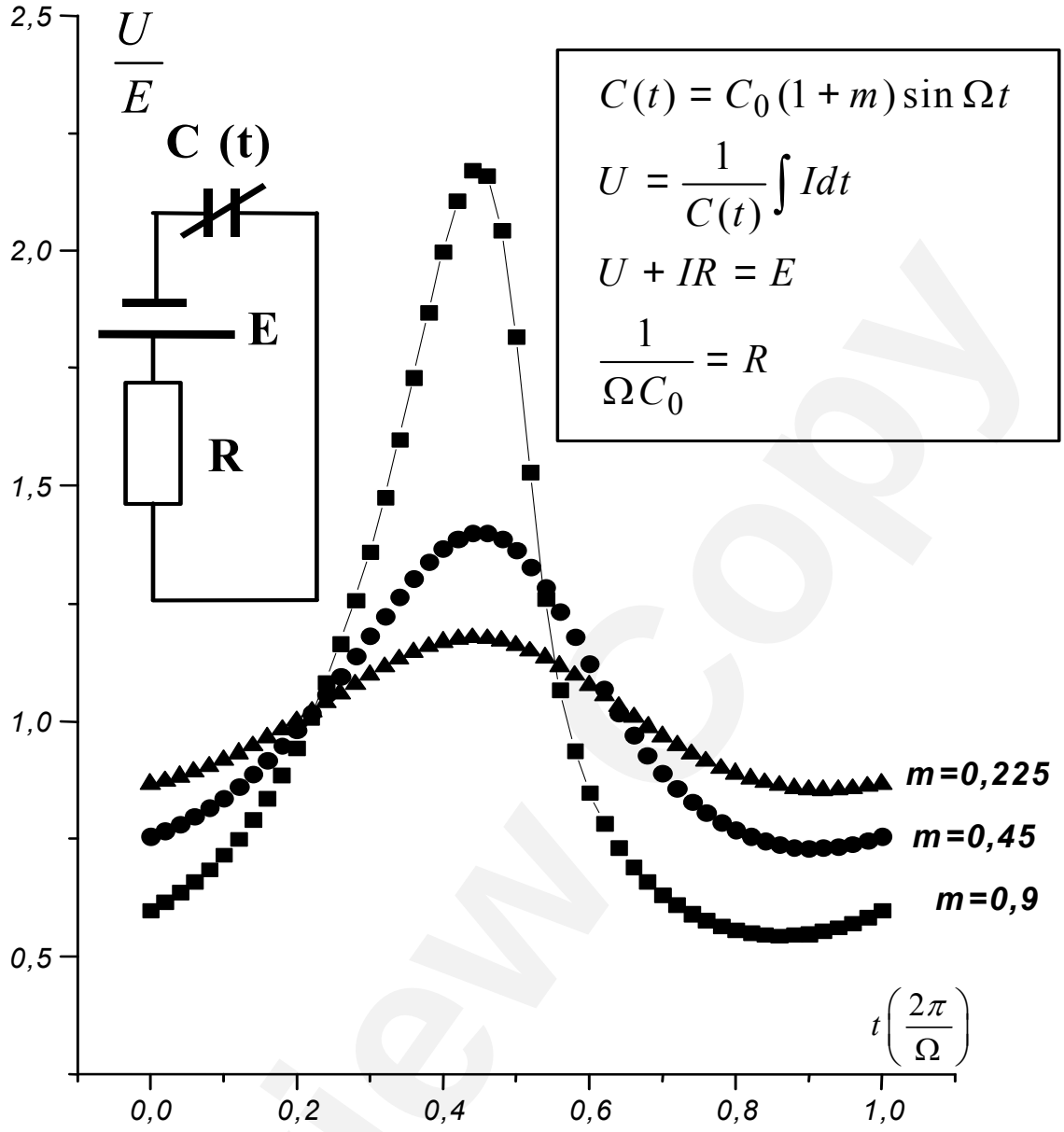

Fig.18 Ioffe V M "New varactors……"

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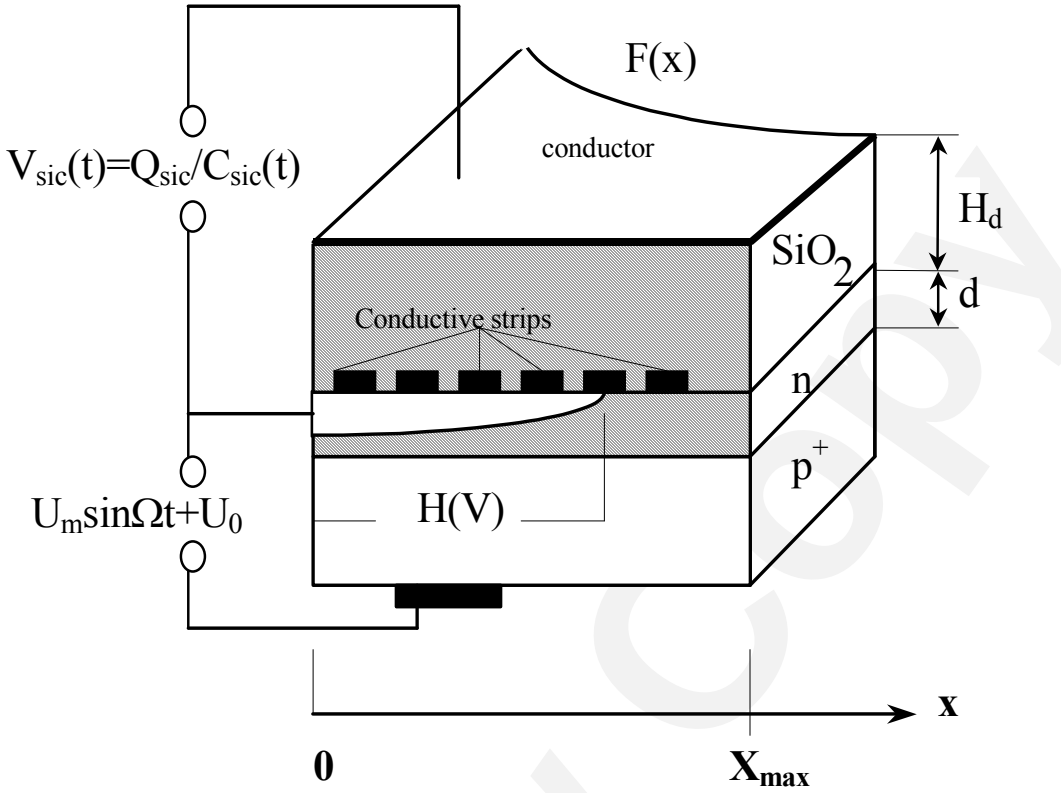

Fig.19 Ioffe V M "New varactors……"

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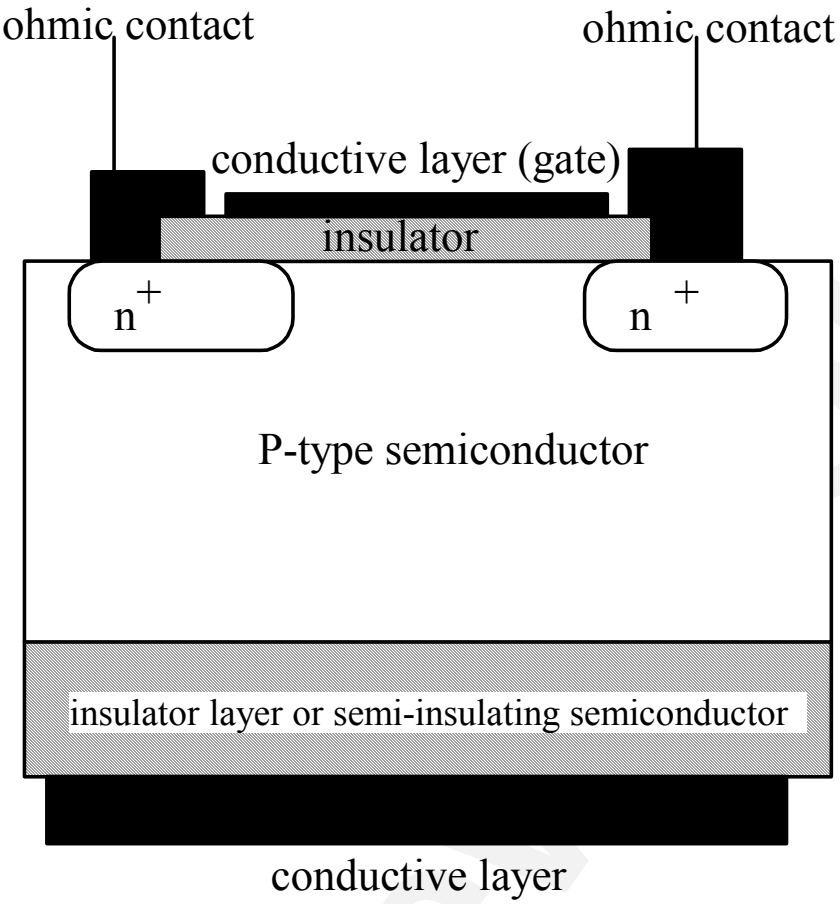

Fig.20 Ioffe V M "New varactors……"

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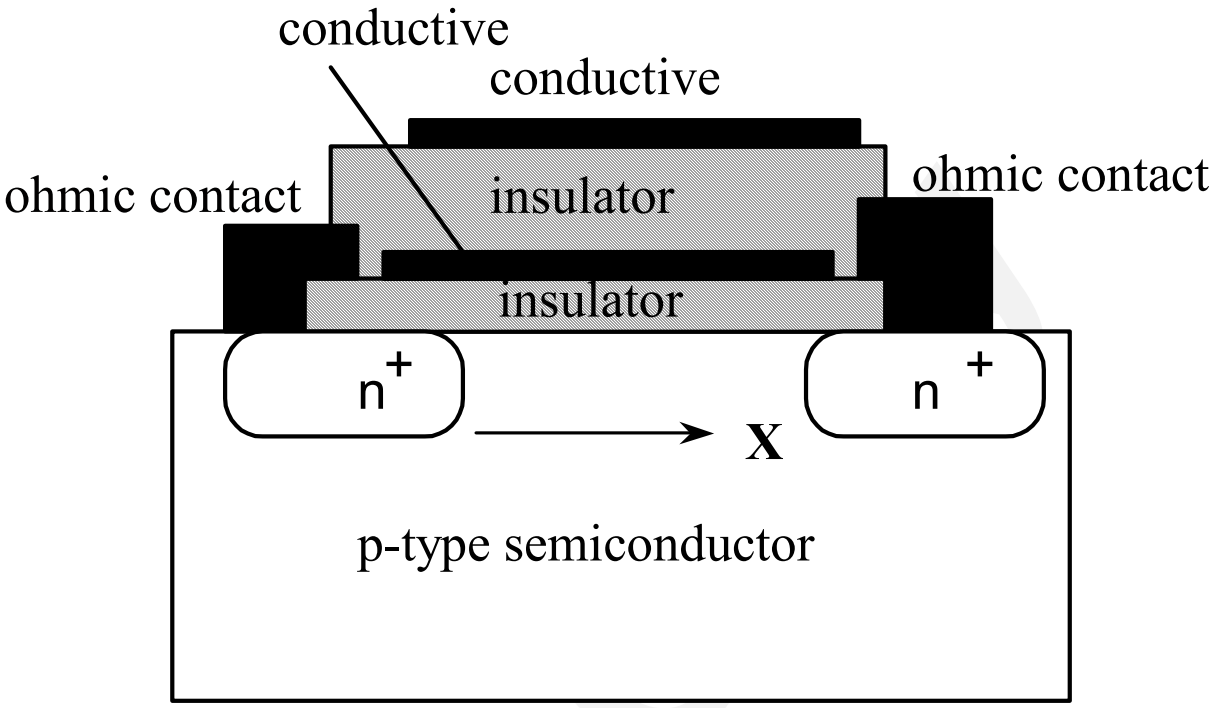

Fig21 Ioffe V M "New varactors…."

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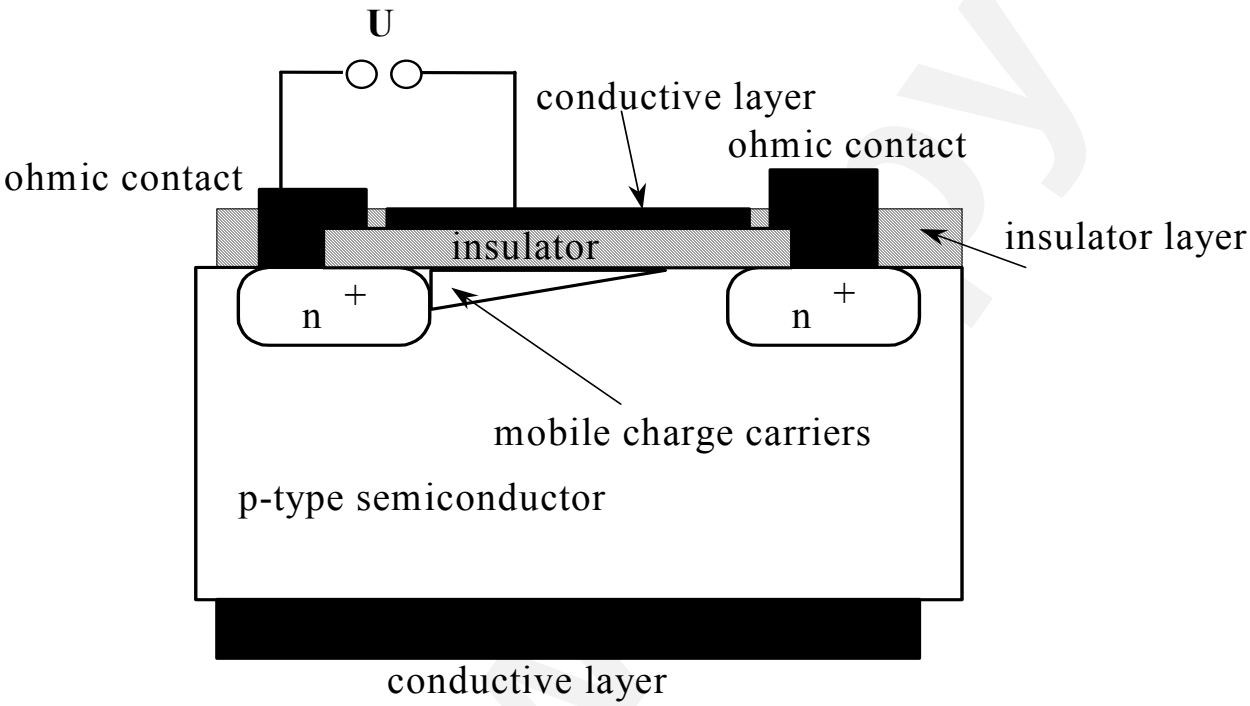

Fig.22 Ioffe V M "New varactors……"

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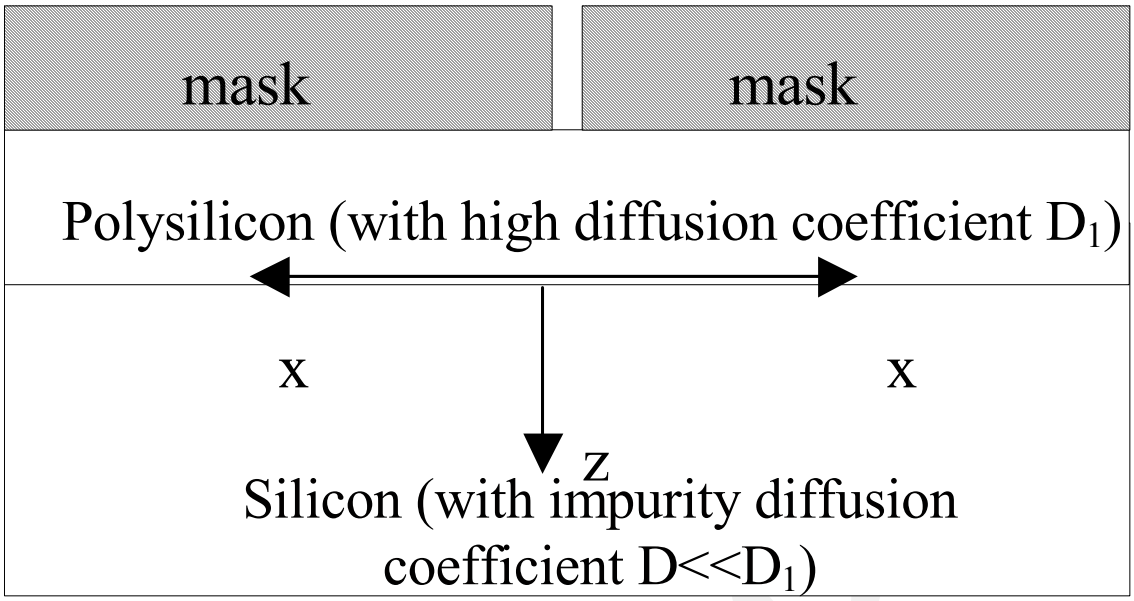

Fig.23 Ioffe V M "New varactors……"

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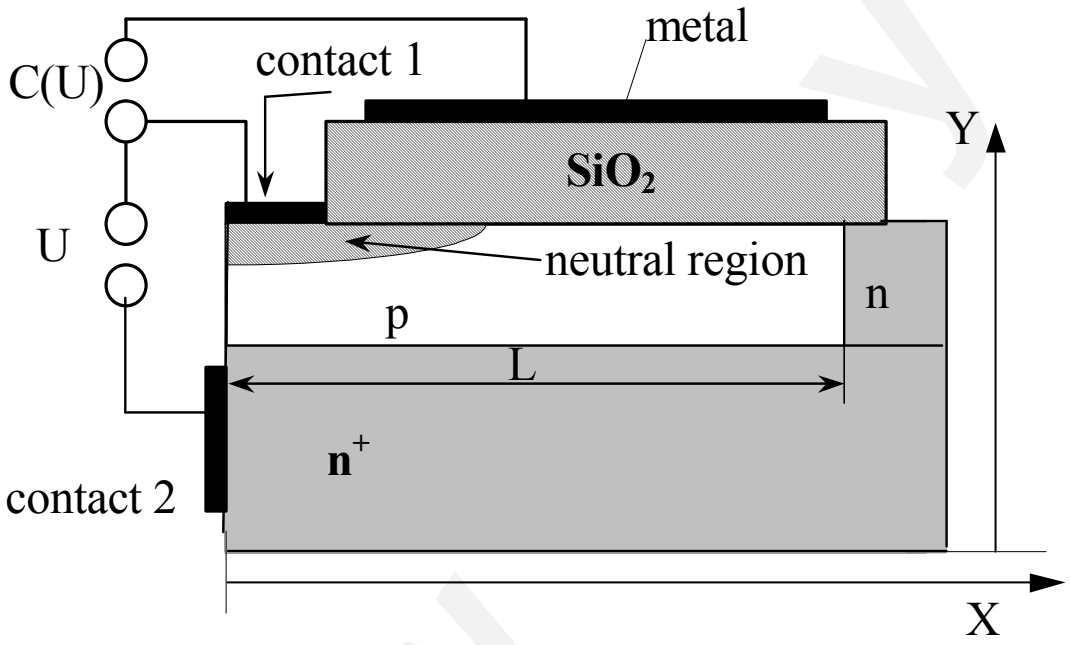

Fig.24(a,b) Ioffe V M "New varactors……"

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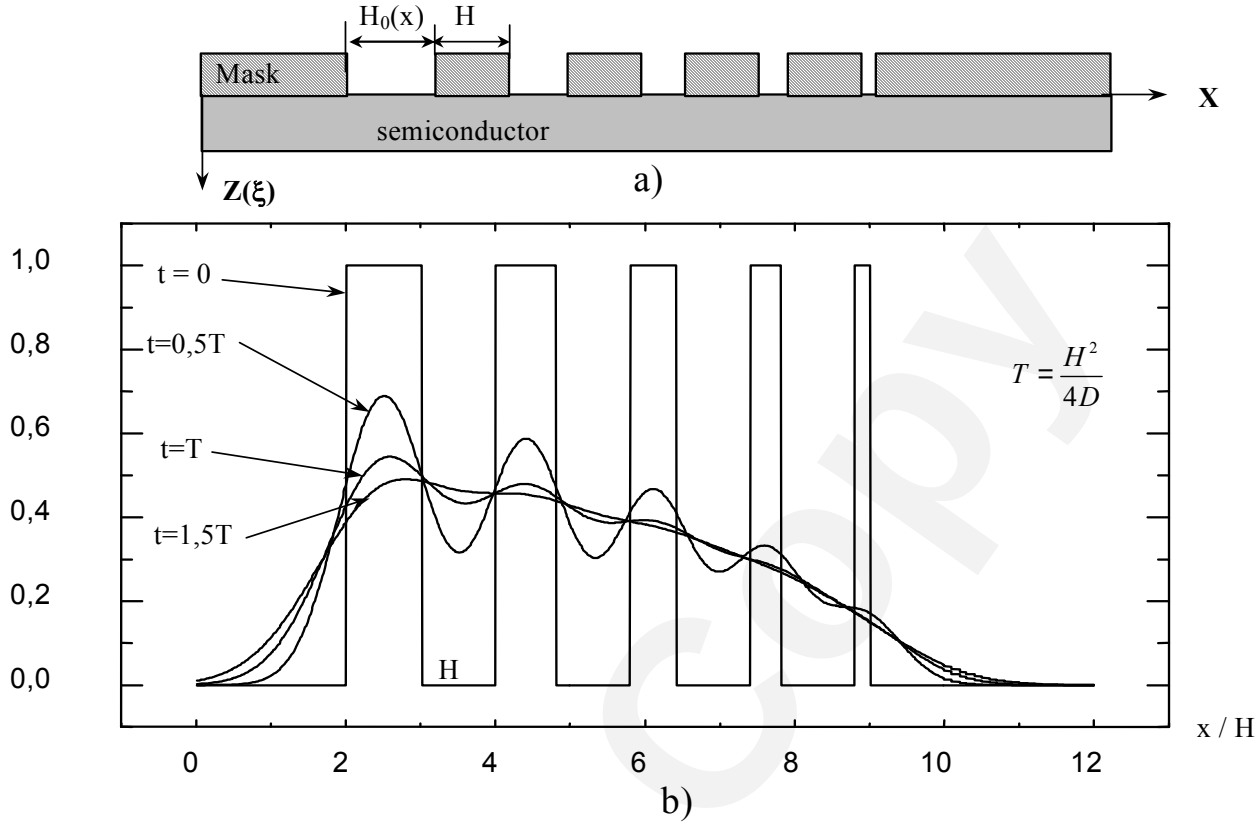

Fig.25 Ioffe V M "New varactors……"

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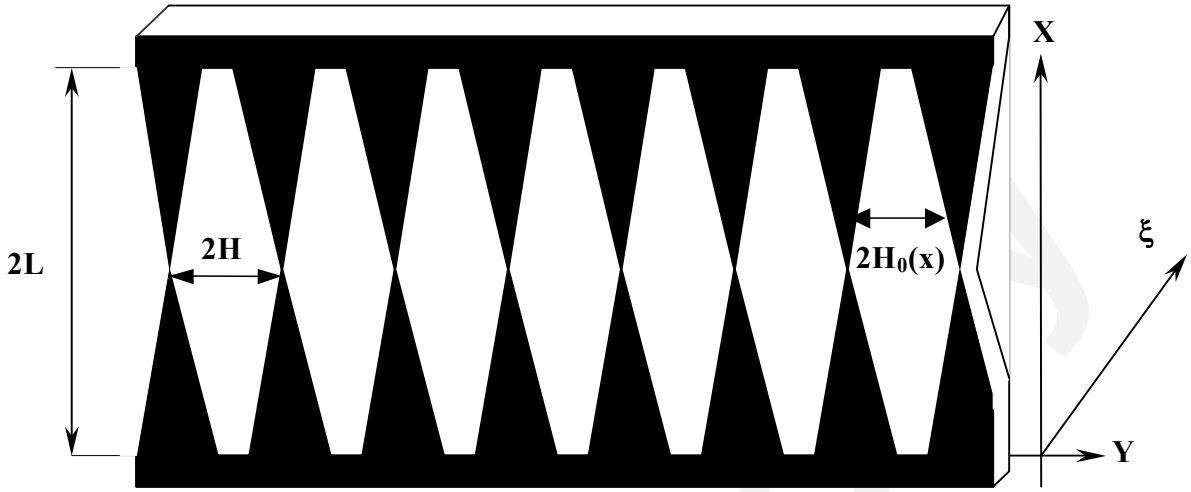

Fig.26 Ioffe V M "New varactors……"

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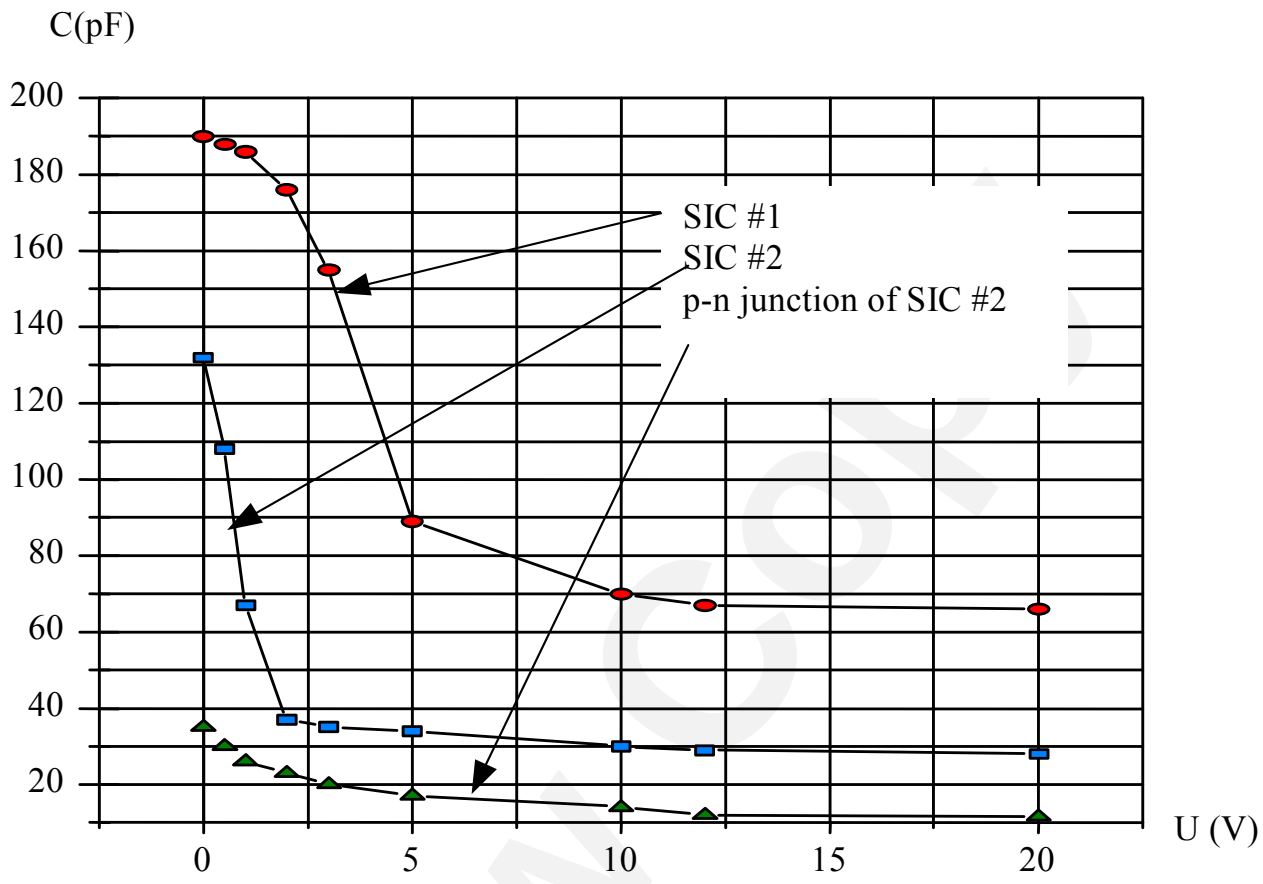

Fig.27 Ioffe V M "New varactors……"

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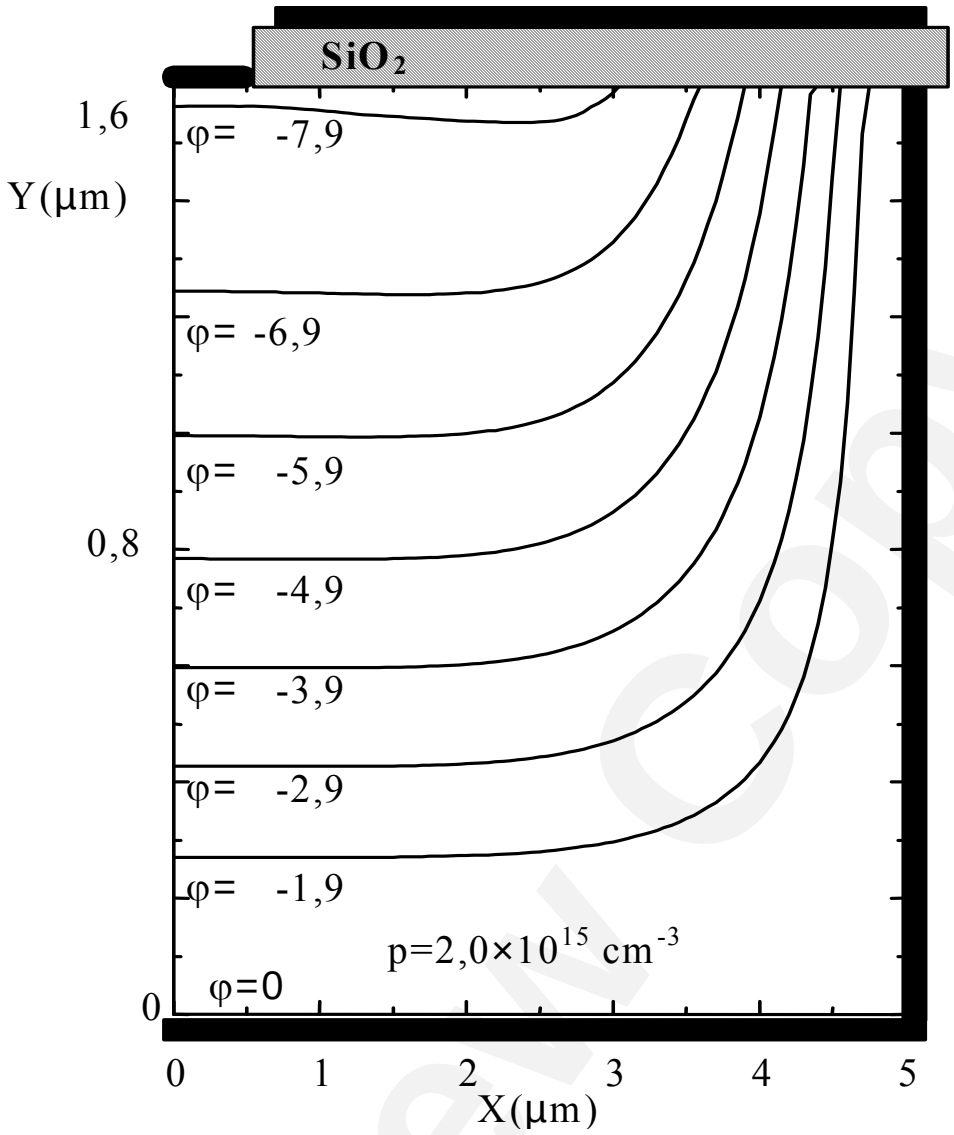

Fig.28 Ioffe V M "New varactors……"

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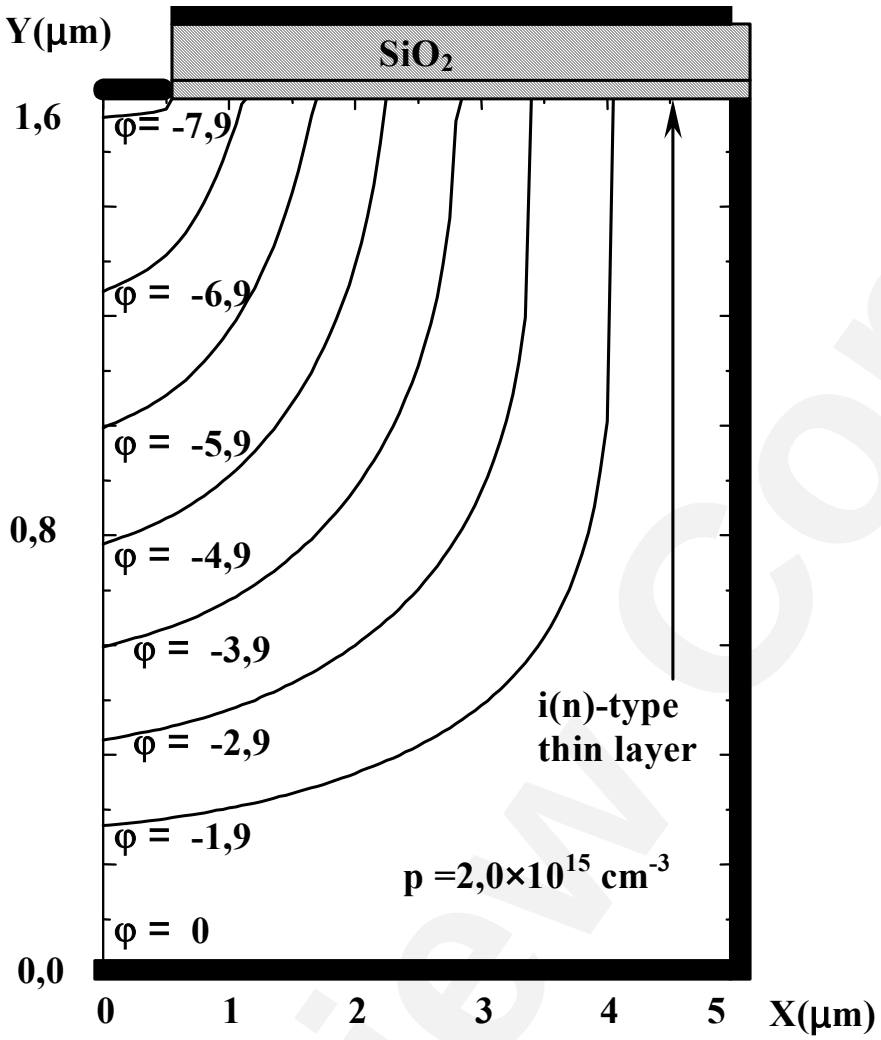

Fig.29 Ioffe V M "New varactors……"

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Fig.30 Ioffe V M "New varactors……"

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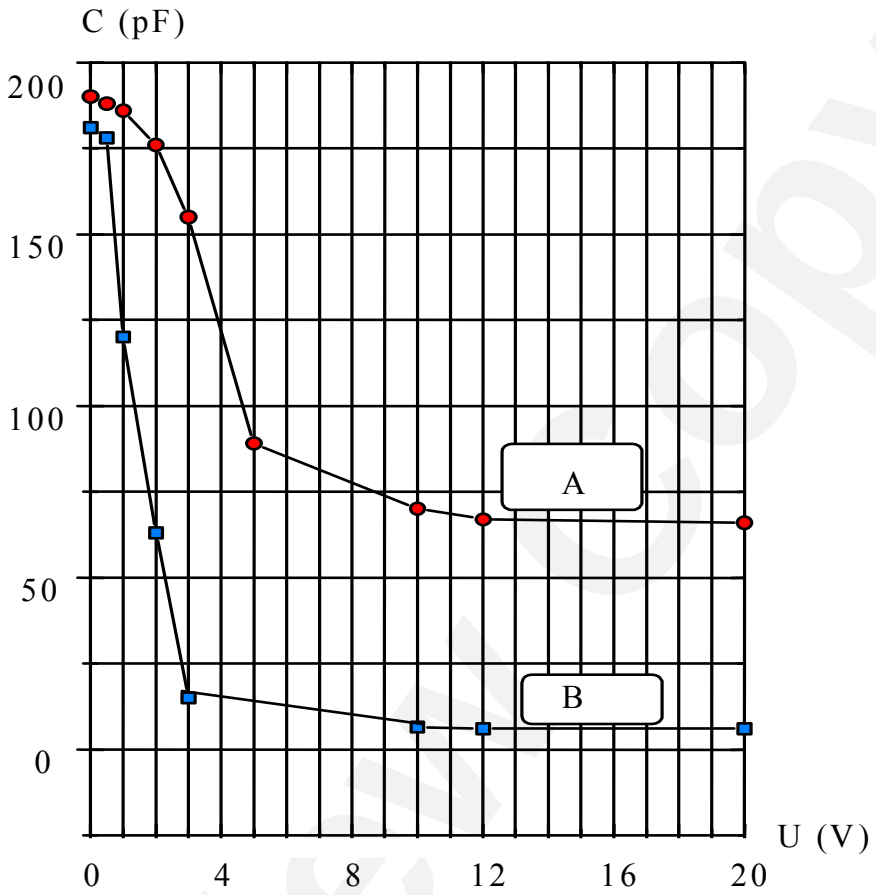

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