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Solid-State Electronics 49 (2005) 385–397
SOLID-STATE ELECTRONICS
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New varactors and high-power high-frequency capacitive devices

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Received 2 April 2004; received in revised form 20 November 2004; accepted 26 November 2004

The review of this paper was arranged by Prof. S. Cristoloveanu

Abstract

A new class of semiconductor devices is proposed with electrically controlled electrode's area. It is shown that by implementing this basic idea within the commonly available technology one is able to construct the varactors (varicaps) with almost any prescribed *C–U* characteristic in contrast to severely limited functionality of traditional devices. More importantly, very promising new devices (which we call semiconductor capacitive transformers—SCTs) can be produced using these varactors. In contrast to known semiconductor devices SCTs are able to overcome the fundamental electronic constraint on the maximum power handling capability, which is currently a real stumbling block for any semiconductor device due to final velocity of mobile charge carriers and junction breakdown. SCT-based ultra-high-power frequency transducers and capacitive transformers can be easily fabricated by means of standard planar technology and are expected to replace bulky inductive transformers in high-frequency and microwave integrated circuits. Also described are some 'proof-of-the-concept' experiments performed by the authors. Results obtained are very encouraging.
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PACS: 85.30.De; 84.30.−r; 85.30.Kk; 73.40.Ty; 66.30.Jt
Keywords: Varactor; Frequency multiplication; Parametric amplifier

1. Introduction

It is now well established that under appropriate bias conditions in all three basic building blocks of present day microelectronics, (p–n junctions, metal-insulator-semiconductor (MIS) structures, and Schottky barriers) a space-charge region (SCR) is formed, which is almost exactly analogous to insulator in usual capacitor, the only difference being that SCR width, *d*, is controlled by the voltage applied, $d = d(U)$.

The effect is known for quite some time and is excellently reviewed in a number of books both from physical point of view [1–3] as well as circuit applications [4]. The shortcomings of any traditional varactor with standard design are well known and seem almost insurmountable. It is widely believed that it is impossible to realize an *arbitrary predetermined* $C(U)$ characteristic because of technological constraints preclude the opportunity to get a predetermined impurity distribution in the body of the device. It is also known that one is unable to realize some practically important $C(U)$ characteristics (for

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doi:10.1016/j.sse.2004.11.018

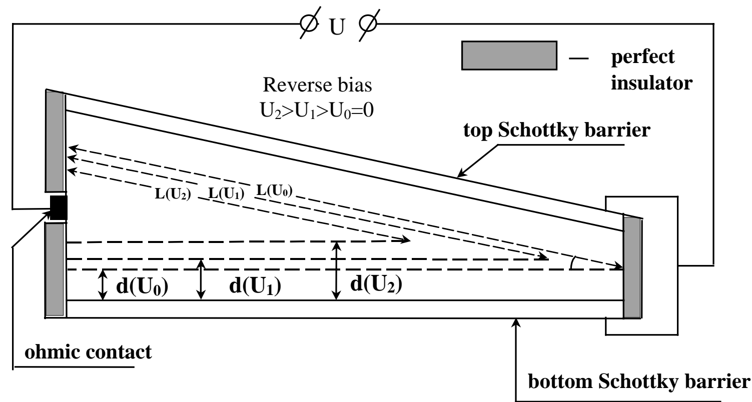

Fig. 1. Non–parallel plate semiconductor capacitance with electrically tuned electrode's area realized on a wedge-shaped sample. $L = L(U)$ and $d = d(U)$ designate effective length of the electrode and space-charge region width for reverse bias U, respectively.

example, *linear*) by means of any impurity distribution within the device body achievable in real practice. It is also evident that a minimum value of varicap capacitance is almost always determined by the breakdown voltage of the junction used, putting thus a fundamental limit on the magnitude of $C_{\min}$.

Our purpose here is to show how these limitations can be removed and to this end in the present work we will show how to make semiconductor capacitances with electrically controlled electrode's area [5], thus adding new and important dimension for device design and implementation.

Most easily one of the ideas behind our approach can be understood with reference to Fig. 1, which shows a cross-section of a wedge-shaped uniformly doped piece of a semiconductor with two Schottky barriers (or homo- or hetero-p–n junctions or MIS structures, as the case may be [6]) formed on its top and bottom surfaces. Also shown in Fig. 1 is the extension of space-charge region under increasing reverse bias. One can see immediately that for this non–parallel plate semiconductor capacitor the effective area of electrodes shrinks progressively under the influence of reverse bias, i.e. we have not only $d = d(U)$, but also $S = S(U)$. This is a *key point* as will become clear below. We, however, would like to warn the reader right from the beginning that in some cases there is no need for wedge-shaped samples or samples with lateral impurity gradients for implementation of the *central idea* (SCT) to be described in Section 3.

The present article is organized as follows. In the next two chapters the principles of operation and some basic implementations are presented for new varactors demonstrating that (in contrast to traditional one's) it is technologically feasible to get almost any desired C–U with very high $C_{\max}/C_{\min}$ ratio. Simple technological methods for obtaining these varactors are described in part 4. In chapter 3 some possible applications of new capacitive devices are discussed with emphasis on their advantages as compared to other semiconductor devices used for the same purposes. Our aim here is to explain in simple terms the operational principles and practical ways of fabrication of these new devices.

2. Varicaps with prescribed capacitance–voltage characteristics

2.1. Linear varicaps

Obviously, the wedge-shaped samples are not very convenient for planar technology. Fortunately, the basic principle can be easily reformulated and applied within the standard planar mainstream. Fig. 2 shows one possible implementation. On p^+-substrate with back ohmic contact a thin low-doped n-layer is grown with a thickness D. In the active region of the device (defined by $0 \leqslant x \leqslant x_{\max}$, $0 \leqslant z \leqslant F(x)$) a non-uniform donor profile $N_i(x,y)$ is generated using, for example, ion implantation, so that impurity concentration (dose) increases from $x_{\max}$ toward the origin of indicated coordinate system. Active region is supplied by top ohmic contact on its periphery. Outside active area the film thickness and doping level are chosen so that n-type film is fully

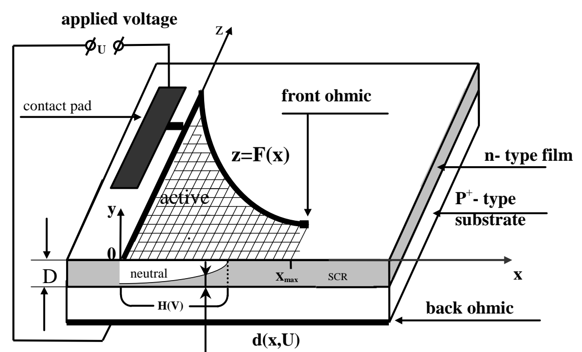

Fig. 2. Planar varactor with electrically modulated electrode's area due to non-uniformely doped active region.

depleted by majority charge carriers. Upon application of reverse bias to film-substrate n–p$^+$ junction the space-charge region (SCR) gradually fills the active volume of the device. Then, both the size of neutral region, $H(U)$, along x-coordinate and effective area, S, of capacitor plate decrease continuously since

$$S = \int_0^{H(U)} F(x)\,\mathrm{d}x + S_{\mathrm{cont}} \tag{2.1}$$

where S_{cont} is the area of the top ohmic contact including contact pad. Now, to obtain the desired $C(U)$ characteristic we have at our disposal two *functions* $F(x)$ and $N_i(x, y)$, which can be varied separately or together, in sharp contrast to conventional varactors whose $C(U)$ depends only on $N_i(x, y)$. In this way we are able to replace a rather intricate technical problem of generating strictly specified impurity distribution within the device body by much simpler task of fabrication of a surface mask with a pre-calculated shape.

Let $d(x, U)$ be the width of SCR at some location x when reverse bias is U (see Fig. 2). Then $d(x, U)$ is given (through double integration of Poisson equation) by

$$U + U_{\mathrm{bi}} = \frac{q}{\varepsilon\varepsilon_0}\int_0^{d(x,U)} yN_i(x, y)\,\mathrm{d}y \tag{2.2}$$

where U_{bi} is the built-in potential of p$^+$–n junction whose dependence on x through $N_i(x, y)$ is here ignored (being almost negligible), and ε is the dielectric constant of semiconductor. Then, obviously (cf. Fig. 2), $H(U)$ can be calculated from

$$d(x, U) = D \tag{2.3}$$

and finally we get for $C(U)$ characteristic of the device

$$C(U) = \varepsilon\varepsilon_0\int_0^{H(U)} \frac{F(x)}{d(x, U)}\,\mathrm{d}x \tag{2.4}$$

Using Eqs. (2.2)–(2.4) one can easily calculate the *lateral shape* $F(x)$ (i.e. masking pattern) of the active region for almost *any* prescribed $C(U)$ with almost *any* $N_i(x, y)$ within active volume of the device. This, apparently missed extra degree of freedom, is of great importance for the whole range of varactor applications.

But first of all, we would like to consider varicaps with *strictly linear* C–U characteristics *over all working* range of applied biases (varicaps with *approximately linear* $C(U)$ characteristics for a *limited range* of reverse biases are known for more than 40 years [4]). As a matter of fact, it can be shown analytically that for clino-varicaps the linear C–U characteristic can be obtained only for about 66% of their working bias range.

As is well known, for frequency multiplication [4] and parametric amplification [7] *linear* varactors are indispensable, simply because for these devices the average capacitance is independent on the amplitude of harmonic signal. As a result, there is no detuning in resonant circuits *if* (non-existent up to now) *truly linear* varicaps are used. The same useful property is obtained for varicaps with symmetrical $C(U)$ characteristic (see e.g., Refs. [8–10]), but, nonetheless, linear varicaps are preferential in some applications.

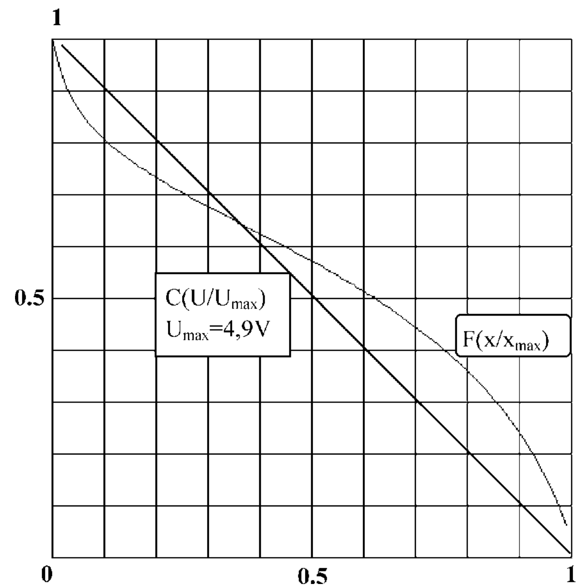

Fig. 3. Calculated shape of the active region for linear varicap.

Fig. 3 presents specific example of the active area shaping [1] for linear varactor fabricated by phosphorus ion implantation (E = 200 keV) into high-purity Si film (0.6 μm thick) with linearly increasing (along x) dose from 1.5×10^{11} ions/cm^2 at $x = x_{\max}$ to 1.0×10^{12} ions/cm^2 at $x = 0$ (see Fig. 2). The layer is grown on degenerately boron-doped ($p^+ = 10^{20}$ cm^{-3}) substrate (the built-in voltage was taken to be U_{bi} = 0.6 V everywhere in the active region).

Device shown in Fig. 2 has an obvious disadvantage, namely, a rather low figure of merit due to large series resistance of neutral volume. It can be, however, eliminated by simply providing on the surface of active region a set of high-conductivity strips along z direction as shown in Fig. 4 [12].

The quality factor Q for varactor without strips (Fig. 2) can be estimated (neglecting reverse current of a p$^+$–n junction) as a ratio of varactor's capacitive resistance to undepleted volume series resistance

$$Q = \frac{1}{\omega CR} \tag{2.5}$$

where ω is the angular frequency of the driving voltage. If ρ_{av} is the average specific resistivity of the neutral part

[1] Idea of shaping of the active volume of the varicap in order to obtain something useful in its C–U characteristic is by no means new. See, for example, Ref. [11] where 'pagoda'-shaped varactors are described. Our approach, however, is much more powerful being planar at the same time.

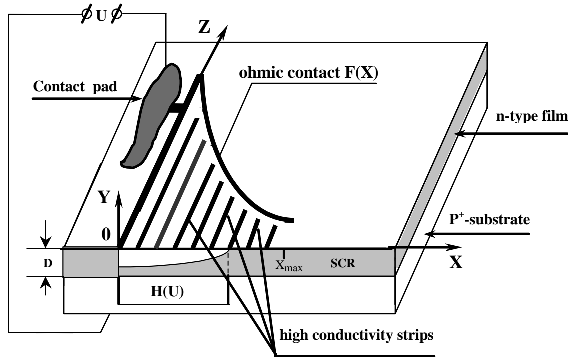

Fig. 4. Varactor with highly conductive stripes on the surface of the active region, which are used to provide an enhanced quality factor of the device.

of the active volume and F_{av} is the average value of $F(x)$ over the $0 \leqslant x \leqslant H(U)$ interval than for $H(U) \gg F_{av}$ we have

$$R \approx \frac{F_{av}\rho_{av}}{DH(U)} \tag{2.6}$$

and

$$C \approx \frac{\varepsilon\varepsilon_0(F_{av}H(U) + S_{cont})}{D} \tag{2.7}$$

If, furthermore, $S_{cont} \ll F_{av}H(U)$, we obtain

$$Q \approx \frac{1}{\varepsilon\varepsilon_0\rho\omega}\left(\frac{D}{F_{av}}\right)^2 \tag{2.8}$$

Consider now the quality factor for the device with strips (Fig. 4). When $H(U) \ll F_{av}$ one can write

$$R \approx \frac{\rho_{av}\Delta}{DH(U)} \tag{2.9}$$

Δbeing the gap between strips and ohmic contact. So, we obtain

$$Q \approx \frac{D^2}{F_{av}\Delta}\frac{1}{\varepsilon\varepsilon_0\rho\omega} \tag{2.10}$$

Comparing Eqs. (2.8) and (2.10) it is seen that using conductive strips one is able to improve the figure of merit by a factor of $\frac{F_{av}}{\Delta}$, which can be easily made to be about 100 for not too small (high-power) devices.

2.2. Other varicaps

Devices with prescribed $C(U)$ characteristics can also be fabricated using films, which are uniform both in thickness and doping. In that case, however, the substrate must be non-uniformely doped. Details of this implementation can be found in [13]. Also of interest are varicaps, which provide sufficiently large capacitance within a generally quite limited chip area available (cf. [14]). Our approach can easily be adapted for this important task also [5]. Finally we would like to return

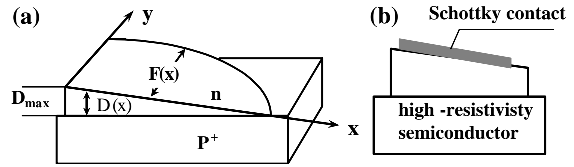

Fig. 5. Clino-varicap fabricated on the wedge—etched n-type epilayer grown on heavily p-doped (a) or semi-insulating (b) substrate.

to wedge-shaped films simply because the first experimental verification of our ideas has been accomplished (in 1994–1995) using exactly that (most difficult and inconvenient) way [15]. Device is fabricated from uniformly doped film grown homoepitaxially on the substrate with opposite conductivity type (Fig. 5(a)) or even insulating (semi-insulating), as the case may be (Fig. 5(b)). Etching can be used for the formation of the wedge-shaped active region. In fact, we simply dip slowly the semi-insulating GaAs substrate with MBE grown n-type epilayer into H_2SO_4–H_2O_2–H_2O etching solution. If the composition of the etching bath and its temperature are held constant, then only dipping rate determines the inclination angle of the wedge, which can be easily controlled to within ±0.1°. Then, the shape of the top Schottky contact can be calculated for almost *any* desired $C(U)$ characteristic. Examples are presented in Fig. 6 for $C/C_{max} \sim (1 - V/V_{max})^n$ with $n = 1, 2, 3$. Certainly, photolithography on the wedge-shaped samples is far from being trivial but, nonetheless, can be performed (painstakingly!), if inclination angle is small enough (and personal is sufficiently skilful and patient). The (root-mean-square) deviation from *designed linear capacitance–voltage characteristic* was measured to be less than 5%, which certainly confirmed our expectations.

Now we can go to the *main topic* of the present work.

3. Semiconductor capacitive transformer

From a circuit designer's point of view any diode is no more than a non-linear resistor whereas a transistor is simply a voltage-controlled non-linear resistor—its output impedance is controlled by input signal. Quite similar to these trivial facts, a semiconductor capacitive transformer (SCT) is a device whose output capacitance is controlled by a signal applied to the input [16–19]. So, in contrast to varicap (or varactor), which usually has only two external leads (see, however, [20,21]) SCT is a three- (or more)-terminal device. Due to this special feature we envisioned that application field of SCTs is vastly expanded in comparison with application field of traditional varicaps (in approximately the same ratio as application range of transistors exceeds that of diodes).

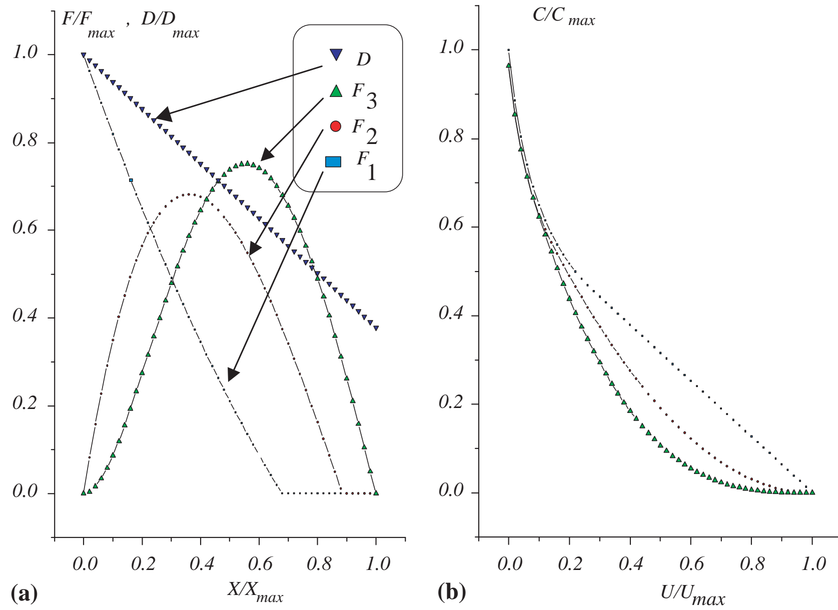

Fig. 6. The shape of the active region for various $C(U)$ characteristics of clino-varicaps with sufficiently small inclination angle (when $\sin\alpha \sim tg\alpha \sim \alpha$) (a) and corresponding capacitance–voltage curves (b). $F_1(x)$ for $C/C_{\max} \sim 1 - V/V_{\max}$, $F_2(x)$ for $C/C_{\max} \sim (1 - V/V_{\max})^2$, $F_3(x)$ for $C/C_{\max} \sim (1 - V/V_{\max})^3$.

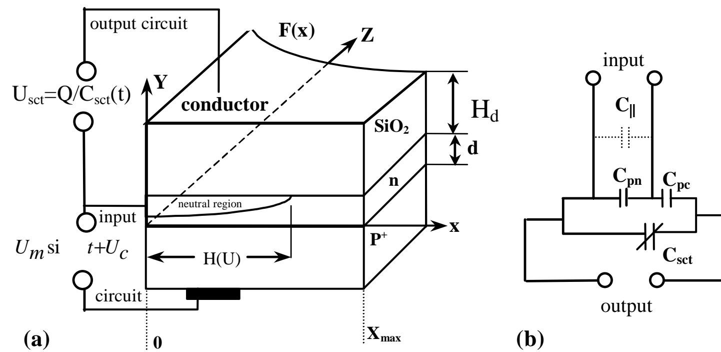

Fig. 7. General outline of semiconductor capacitance transformer (a) and its simplest equivalent circuit (b).

Semiconductor capacitive transformers can be used for amplification and frequency transformation and are highly superior to transistors as concerns the useful power delivered to the external load since temperature constraints are greatly reduced (capacitors are heated only in the inverse proportion to their Q-factor) and the so called electronic constraint, routed in breakdown voltage of any semiconductor junction [2] is almost *completely eliminated* in the SCTs. Semiconductor capacitive transformers fit nicely into existing integrated circuit technology. Moreover, capacitance transformers are highly preferential against usual inductive transformers from both technological and economic viewpoints and, we believe, could replace them at least in high-frequency (and even microwave) range.

3.1. SCT operational principle explained

Let us consider a capacitance transformer (SCT) comprising a p–n junction with n-layer doped non-uniformely along x-coordinate (see Fig. 7). On the top surface of this p–n junction a dielectric layer is grown having a metallic electrode thereon. Both n and p regions are provided with ohmic contacts so that a reverse bias can be applied to the p–n junction. Let doping concentration in the active region of n-layer $N_i(x, y)$ (where $0 \leqslant x \leqslant x_{\max}$, $0 \leqslant z \leqslant F(x)$, and $y \leqslant d$) increases in some predetermined manner from $x_{\max}$ toward 0. Then, with increasing reverse bias the neutral (undepleted) region, $H(U)$, would shrink and effective area of SCT electrodes (between neutral region and metallic overlayer) would

[2] Exactly this is a reason that a maximum power delivered by any semiconductor device to the external circuit is inversely proportional to the square of operating frequency.

also decrease. Thus, we see that concurrently with usual drop of p–n junction depletion capacitance to which bias is applied, another capacitance changes—that between undepleted part of n-layer under dielectric and metal film. It is exactly this capacitance, which is a hart of SCT (see Fig. 7(a)). If $C_{SCT}(t)$ is time-dependent capacitance of SCT, Q_{SCT} is the charge on SCT electrodes, then voltage on SCT will be given by

$$V_{SCT}(t) = \frac{Q_{SCT}}{C_{SCT}(t)} \tag{3.1}$$

So, applying a voltage to the contacts of semiconductor junction we can control the voltage on the SCT. Evidently, the charge to the SCT can be supplied through the load from external source (dc and/or ac). In that case the current and voltage on the load are controlled by input SCT signal, quite similar to transistor or electron tube. Note also that SCT can be fabricated from any varactor, if additional insulating layer is formed on its surface with metallic electrode on top.

First of all, however, one *extremely important feature of newly proposed device should be emphasized*. The point is that SCT is inherently able to overcome a very fundamental constraint of each and every current semiconductor device, namely, the so-called "electronic constraint" on the maximum power deliverable to external circuit. The constraint mentioned stems directly from the fact that under the influence of applied bias (direct or reverse) the space-charge layer thickness is changed in the device. If, for example, we wish to extract the highest possible power from a bipolar transistor, then the voltage in the output (collector) circuit ought to be varied within the largest possible margins, i.e. from full depletion (never achievable in practice) to full neutrality (also never achievable). But saturated electron drift velocity (V_s) does not allow accomplishing the voltage variation instantaneously, and we conclude that a thickness of the collector is limited (at high-frequencies, f) to the value of about $\frac{V_s}{f}$. If the collector is thicker, than additional ohmic losses are inevitable. In its turn, the breakdown voltage of that junction limits the maximum voltage applied to base-collector interface. It follows immediately that maximum power developed on the load is of the order of

$$P_{max} \approx \left(E_{bd}\frac{V_s}{f}\right)^2 \frac{1}{R} \tag{3.2}$$

where E_{bd} is the breakdown electric field of the junction concerned and R is the load resistance. These considerations are *quite general and may be applied to any semiconductor device*.

The SCT is free from this constraint (at least, as output circuit is concerned) and its output power is determined only by Q-factor of the system. Thus, it allows to easily transformate the low-power low-frequency input signals into high-power high-frequency output. In that respect, we believe, the SCT *is second to none* in the field of semiconductor electronics. The output circuit of SCT-based frequency transducer is drived by alternating current of relatively low frequency, which is transformed into high-frequency signal in the same circuit.

As is shown in Fig. 7(a) we have a low power high-frequency source in the input circuit of the device. In order to minimize the output/input cross-talk one can increase a thickness, H_d, of insulating layer and/or to put additional capacitor ($C_{\parallel}$) in parallel to semiconductor junction (see Fig. 7(b) depicting equivalent circuit of the device). From theory of parametric amplifiers it is well known that amplifier is most effective when

$$mQ \approx 1 \tag{3.3}$$

where m is the capacitance modulation coefficient and Q is the quality factor of the circuit containing capacitance being modulated. At first glance, it seems that an increase in insulator thickness (H_d) would inevitably result in substantial worsening of the modulation coefficient and, as a consequence, in poor device performance at high frequencies. Contrary to common sense expectations, we will show below that mQ product is, in fact, independent of insulator thickness for *properly* designed SCT.

To obtain simple analytical estimates let us consider Fig. 8, which represents SCT device having a grid-like ohmic contact fabricated on n-type layer (period a, metal stripe width a_1) with an insulating layer (i-layer) on top. By the way, this i-layer can be fabricated separately and simply pressed onto main device body.

In this device the tuning range ($K = C_{max}/C_{min}$) is obviously reduced for thick i-layer. Let us calculate the C_{min}. In the literature [22] one can find the solution for analogous problem expressed through the elliptical functions, but the results obtained (or their approximations expressible through the elementary functions [23]), are not reproduced here, since application of these bulky formulae to the case at hand is too lengthy and, in fact,

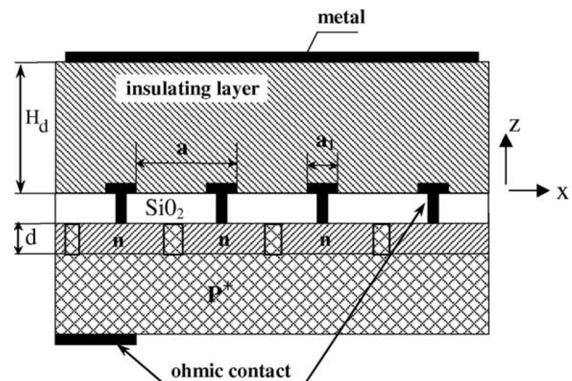

Fig. 8. Cross-section of the SCT with grid-like ohmic contact to partitioned n-type active layer (as used for estimation of mQ product).

unnecessary. Our solution given below is much shorter and, at the same time, is sufficiently accurate for engineering estimates.

For $H_d \gg a \gg a_1$ (where H_d is the dielectric layer thickness, see Fig. 8) the potential in the arbitrary z-plane cross-section of the insulator is a sum of the grid potential (with a period a along x-coordinate) and potential of the top-most metallic electrode. It can be written as

$$\varphi = A\cos\left(\frac{x}{2\pi a}\right)\exp\left(-\frac{z}{2\pi a}\right) + \frac{\delta}{\varepsilon}(z - H_d) \tag{3.4}$$

The first term in this expression describes the periodic potential originated from the grid, whereas the second term pertains to the potential induced by top electrode. By direct substitution one can confirm that (3.4) is a solution of the Laplace equation. In (3.4) δ is the surface charge density, ε is the dielectric constant of the insulating layer, and A is a constant. The parameters A and δ must be determined from boundary conditions. If $a \ll H_d$ the first term is vanishingly small and $\varphi = 0$ for $z = H_d$. When $z = 0$ (with $\cos(\frac{x}{2\pi a}) = -1$) we have for the potential of the contact

$$\varphi = A + H_d\frac{\delta}{\varepsilon} \tag{3.5}$$

Periodic contact arrangement corresponds to an extremum of (3.4) at $z = 0$ because contact's potential is a constant and any function variation near its extremum can be safely neglected. Differentiating (3.4) by z at $z = 0$ (with $\cos(\frac{x}{2\pi a}) = -1$) and taking into account that potential near grid is a sum of grid potential $= \frac{1}{2}\frac{a}{a_1}\frac{\delta}{\varepsilon}$ and the top electrode potential $= \frac{1}{2}\frac{\delta}{\varepsilon}$ one obtains

$$\frac{A}{2\pi a} + \frac{\delta}{\varepsilon} = \frac{1}{2}\frac{a}{a_1}\frac{\delta}{\varepsilon} + \frac{\delta}{2\varepsilon} \tag{3.6}$$

From this we have

$$A = \pi\left(\frac{a\delta}{a_1\varepsilon} + \frac{\delta}{2\varepsilon} - \frac{\delta}{\varepsilon}\right) = \pi a\frac{\delta}{\varepsilon}\left(\frac{a}{a_1} - 1\right) \tag{3.7}$$

Since

$$C_{\min} \sim \frac{\delta}{\varphi} \sim \frac{\varepsilon}{H_d}\frac{1}{1 + \frac{\pi a}{H_d}\left(\frac{a}{a_1} - 1\right)} \tag{3.8}$$

and

$$C_{\max} \sim \frac{\varepsilon}{H_d} \tag{3.9}$$

the tuning range $K = C_{\max}/C_{\min}$ is given by

$$K = 1 + \frac{\pi a}{H_d}\left(\frac{a}{a_1} - 1\right) \tag{3.10}$$

If, in parallel with p–n junction, a large capacitor ($C_{\|}$) is switched in, we can write

$$K = \frac{2}{1 + \frac{1}{1 + \frac{\pi a}{H_d}\left(\frac{a}{a_1} - 1\right)}} \tag{3.11}$$

For this case Q-factor and the maximum modulation coefficient m can be expressed as

$$Q \approx \frac{H_d d}{\varepsilon\rho\omega(a - a_1)}; \quad m_{\max} \approx \frac{K-1}{K+1} \approx \frac{\pi a}{2H_d}\left(\frac{a}{a_1} - 1\right) \tag{3.12}$$

where ρ is the average resistivity of the active n-layer. From (3.12) one can see that a product $m_{\max} Q$ is indeed independent from H_d. Note also that in parallel-plate capacitor approximation one can write if $a_1 \gg H_d$

$$K = \frac{a}{a_1}; \quad m_{\max} = \frac{\left(\frac{a}{a_1} - 1\right)}{\left(\frac{a}{a_1} + 1\right)}$$

If $C_{\|}$ is used one have

$$K = \frac{a}{2a_1}; \quad m_{\max} = \frac{\left(\frac{a}{2a_1} - 1\right)}{\left(\frac{a}{2a_1} + 1\right)}$$

The device presented in Fig. 8 allows (when $a \ll d$) to use n-layers for which the pinch-off voltage is larger than breakdown voltage and to enhance the Q-factor even further.

It seems that some specific example will be helpful at this point.

3.2. A worked example

Below an estimate of relevant parameters is given for the SCT which can be used as a frequency converter from $f_{\min} = 1$ GHz to $f_{\max} = 5$ GHz with 200 W peak power delivered (note, that if any of the existing varactors is used for the same purpose the power available will be at least *two orders of magnitude* lower).

Applied to the p–n junction is a signal with $f_{\max} - f_{\min} = 4$ GHz, whereas to SCT a signal with $f_{\min} = 1$ GHz is applied, and a tuned resonance circuit with a resonance frequency $f_{\max} + f_{\min}$ is used. An estimation of the SCT basic parameters proceeds then as follows:

1. Contact grid period must obey the obvious constraint

$$a < \frac{V_s}{f_{\max} + f_{\min}} = \frac{1 \times 10^5\ \text{ms}^{-1}}{6 \times 10^9\ \text{s}^{-1}} \approx 17\ \mu\text{m} \tag{3.13}$$

where V_s is the saturated electron drift velocity in Si (taken to be $= 1 \times 10^5$ m s^{-1}).

2. Let the insulating layer be fabricated from quartz (with a breakdown electric field E≈10^9 Vm^{-1}) and let a thickness of this layer to be about 100 μm. Then,

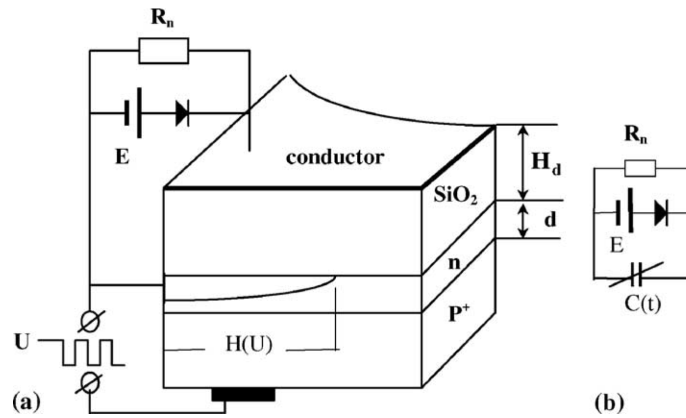

Fig. 9. Capacitance transformer with DC voltage supply and a diode. General outline (a) and equivalent circuit (b).

$$K = \frac{2}{1 + \frac{1}{1 + \frac{\pi a}{H_d}\left(\frac{a}{a_1} - 1\right)}} \approx 1.4 m_{\max} \approx \frac{1 + K}{1 - K} \approx 0.2 \quad (3.14)$$

3. The horizontal dimension of n-base (a_x) can be chosen from the condition

$$a_x = \frac{\lambda}{20} = \frac{c}{20 f_{\max}\sqrt{\varepsilon}} \approx 1.5 \text{ mm} \quad (3.15)$$

the maximal capacitance being then

$$C_{\max} = \frac{2\varepsilon a_x^2}{H_d} \approx 1.5 \times 10^{-12} \text{ F} \quad (3.16)$$

4. The doping level of n-base can be varied in a wide range. Let us choose the thickness of n-base to be 1 μm with doping level of $n = 7 \times 10^{15}$ cm^{-3}.
5. To find a maximum voltage to be applied to SCT and a minimum value of the capacitance ($C_{\parallel}$) to be switched in parallel with p–n junction, let us assume that a fraction of voltage, which drops on p–n junction, is 1 V. Then,

$$U_c = \frac{2PQ}{f_{\min}\sqrt{0.5 C_{\max}}} \approx 1000 \text{ V} \quad (3.17)$$

and for $Q = 10$, $P = 200$ W one finally obtains

$$C_{\parallel} = \frac{0.5 C_{\max} \times U_c}{1V} = 7.5 \times 10^{-10} \text{ F} \quad (3.18)$$

In this way, all relevant parameters of SCT-based frequency converter are now estimated.

3.3. Other circuit configurations with SCTs

Here we would like to mention a couple of different configurations for circuit usage of SCTs. Referring to Fig. 9 (proposed by A. Maksutov) one can see that applying a reverse bias pulse to the p–n junction we can decrease the relevant capacitance (i.e. a capacitance between n-layer and top-most metal film), thus forcing the voltage on SCT to increase (see (3.1)). As a result the diode will be blocked and the SCT would discharge through the load resistance R_n. The maximum voltage on SCT is given by

$$U_c \approx E\frac{C_{\max}}{C_{\min}} \quad (3.19)$$

where E is the magnitude of the (constant) supply voltage, and $C_{\max}(C_{\min})$ is the maximum (minimum) of device capacitance.

Fig. 10 shows capacitance transformer containing high constant voltage source (E) with a load resistor (R), connected to n-layer and aluminum metallization of SCT. The input signal $U = U_m \sin \Omega t + U_c$ is applied to p–n junction. Under the influence of comparatively small input signal the SCT will be modulated, being a part of high voltage circuit. The calculated time dependence of SCT voltage for that case is shown in Fig. 11.

3.4. MIS-based SCTs

Semiconductor capacitive transformers can be also fabricated using metal-insulator-semiconductor (MIS) structures [24]. In case at hand the principle of SCT operation is closely related to well-known physics

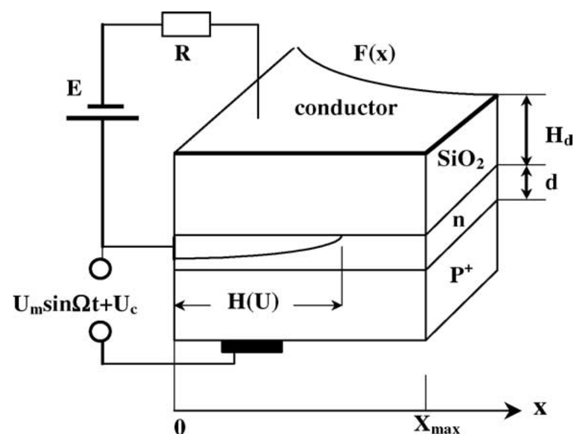

Fig. 10. SCT with high constant voltage supply.

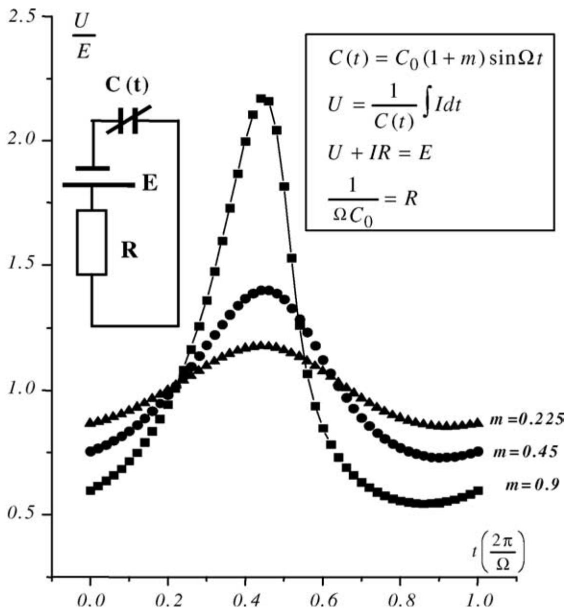

Fig. 11. SCT voltage for the device shown in Fig. 10 for different values of capacitance modulation coefficient. Inserts show an equivalent circuit (left) and equations used for calculation of the curves (right).

of normally "off" MIS transistors [3]. Consider, for example, Fig. 12, which shows a typical p-MISFET with substrate back surface provided by additional insulator layer coated by conductive (metallic) film. If positive bias is applied between the gate and anyone of the ohmic contacts, an inversion channel can be formed under the gate dielectric. As a result, the capacitance between ohmic contacts and bottom-most electrode (SCT!) will change. Obviously, high-resistivity semiconductor can be used as a bottom quasidielectric for frequencies

$$\omega \leqslant \frac{1}{\varepsilon_0 \varepsilon \rho} \tag{3.20}$$

where ρ is the resistivity of the semi-insulating semiconductor.

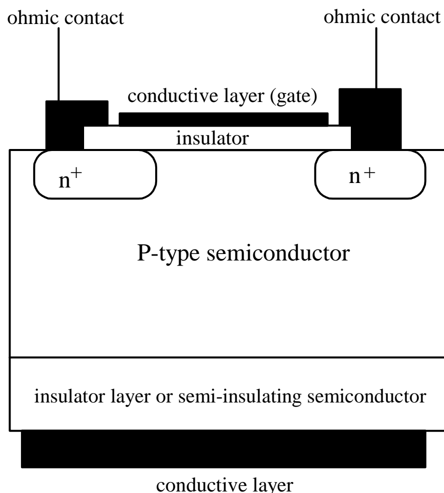

Fig. 12. Double-gated MISFET-based SCT.

If semiconductor under gate dielectric (between source and drain) is doped non-uniformely along x-coordinate, then shaping the device active area allows one to vary SCT in a predetermined way. Evidently, source and drain contacts can be short-circuited but availability of *two* contacts is beneficial since transient processes of carrier dissipation are facilitated, which can be important for high-frequency applications.

4. Experimental

4.1. The first experience of SCT fabrication

In order to fabricate sufficiently flexible semiconductor capacitance transformer one must be able to generate a laterally non-uniform impurity distribution under the gate in a controlled manner. In principle, focused ion beam implantation is uniquely suited for that purpose. The technique, however, was unavailable for us and we were forced to devise and use another approach.

Laterally inhomogeneous (but programmed!) impurity profiles have been created by implanting and subsequent diffusion of dopant atoms through the system of variable—width openings in SiO_2 masking layer. The idea is illustrated by Fig. 13, more details may be found in [25].

We have fabricated the device shown schematically in Fig. 14. The main body of the device consists of p-base (with an area 0.6–1.0 mm^2) having laterally non-uniform doping so that the acceptor concentration decreases from left to right. The length (L) of p-base along x-coordinate varied from 10 to 50 µm. Two ohmic contacts were fabricated: contact 1 to the active region and contact 2 for n^+-substrate. Gate oxide thickness was 0.2 µm. It was assumed that by increasing the reverse bias applied to p–n junction we could shrink in a controlled fashion the neutral region in the p-base along x-coordinate. Then, simultaneously with usual decrease of p–n junction depletion capacitance, we should observe a corresponding variation in SCT (measured between the gate contact and contact 1).

In our experiments we used the boron doses (E = 100 keV) from 1×10^{12} to 3×10^{12} ions/cm^2, annealing times have been varied from 14 to 30 h and maximum (minimum) window widths used were 7 µm (2.8 µm). Using this approach and the appropriate mask we were able to fabricate a p-base, in which the boron concentration increases almost linearly toward the ohmic contact (contact number 1 in Fig. 14) from beneath the gate.

For device fabrication six silicon wafers were used (n-type, heavily Sb-doped to a concentration of electrons 5×10^{19} cm^{-3} with 12 µm—thick epitaxial layer on top doped to 10^{15} cm^{-3}, also n-type). In general, 12 different

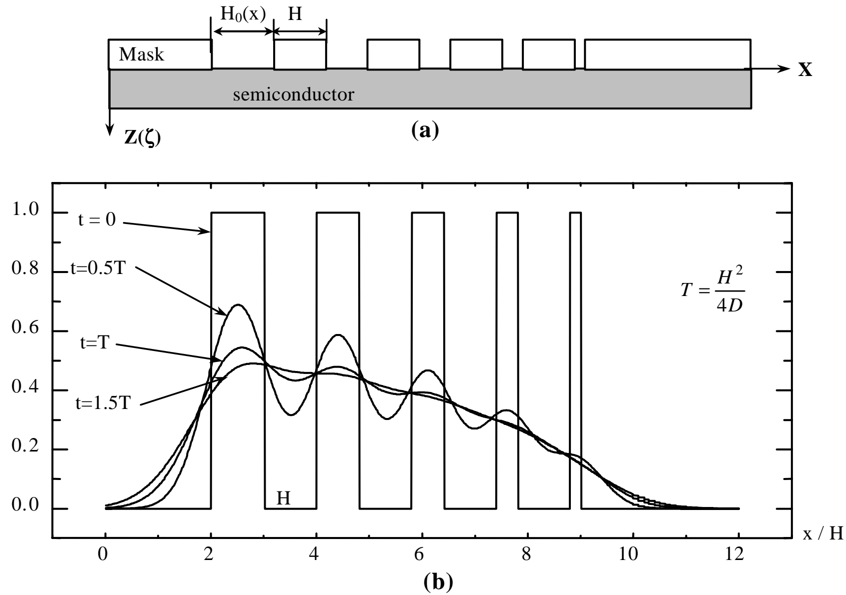

Fig. 13. Diffusion mask configuration (a), and impurity profiles under the mask for different annealing times (b).

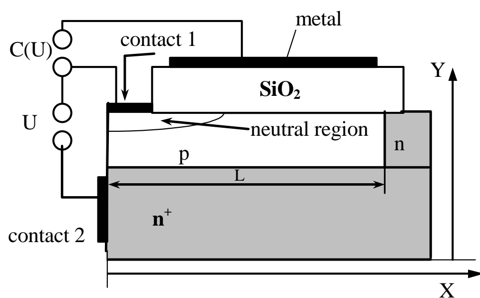

Fig. 14. Schematic representation of experimental device.

non-uniform p-type doping distributions along x-coordinate have been realized and tested in our work.

The pre-calculated value of the punch-through reverse voltage (U_p) for p-base in our devices have been expected to be less than 5 V in all cases:

$$U_p = \max\left\{\frac{q}{\varepsilon_0\varepsilon}\int_0^d N_i(x,y,z)z\,\mathrm{d}z\right\} < 5\ \mathrm{V} \tag{4.1}$$

We expected also that applying higher reverse bias ($U > U_p$) to the p–n junction we can force the space-charge layer to fill the whole body of p-base region and then the minimal value of SCT should be about 4–6 pF (depending on the specific device geometry). Both our expectations fail completely! Experimental C–U measurements indicate that full depletion of p-base is *never achieved for any reverse bias*. Contrary to our expectations a certain fraction (1/3–1/5) of the p-base material remains undepleted even at highest reverse bias used, see Fig. 15. The ratio $C_{\min}/C_{\max}$ was measured to be greater than 1/5, whereas the expected magnitude of this ratio should be less than 1/30. Moreover, the minimum value of SCT was practically independent of the gate voltage.

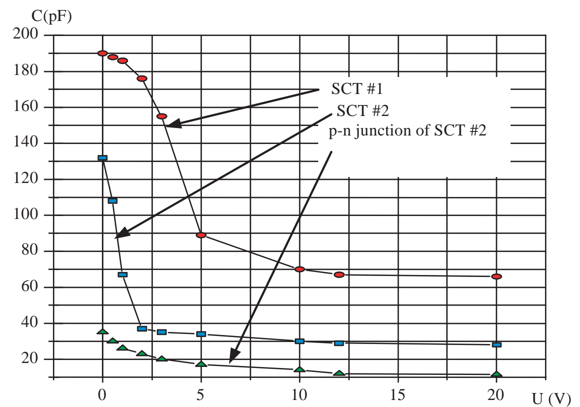

Fig. 15. Typical results of capacitance–voltage measurements.

4.2. Explanation of measured results and refinement of device structure

For the fabrication of varactors and SCTs with a large tuning range ($C_{\min}/C_{\max}$) two questions naturally arise in view of experimental results outlined in the proceeding paragraph:

1. Why full depletion of mobile charge carriers in a p-base region of a device is not achieved?
2. What have to be done in order to obtain the necessary full depletion?

To answer the first question a 2D simulation of our device was undertaken. Within standard drift-diffusion model [26] the following problem has been formulated and solved (see Fig. 16):

$$\nabla^2\varphi = -\frac{q}{\varepsilon_0\varepsilon}(N_\mathrm{d} - N_a + p - n) \tag{4.2}$$

$$J_n = -q\mu_n \nabla\varphi + q\nabla D_n n \tag{4.3}$$

$$J_p = -q\mu_p \nabla\varphi - q\nabla D_p p \tag{4.4}$$

$$\frac{dn}{dt} = 0 = -U + \frac{1}{q}\nabla J_n \tag{4.5}$$

$$\frac{dp}{dt} = 0 = -U + \frac{1}{q}\nabla J_p \tag{4.6}$$

$$U = \frac{np - n_i^2}{\tau_n(p + n_i) + \tau_p(n + n_i)} \tag{4.7}$$

We used the following boundary conditions:

on the first upper ohmic contact (cf. Fig. 16)

$$\varphi = \varphi_1;\ p = p_1;\ n = n_1;\ pn = n_i^2;$$
$$n - p = N_d - N_a; \tag{4.8}$$

on the second ohmic contact, i.e. at the bottom and right-hand boundary of simulation domain (cf. Fig. 16)

$$\varphi = 0;\ pn = n_i^2;\ p = p_1 \exp\left(-\frac{q\varphi_s}{kT}\right);$$
$$n = n_1 \exp\left(\frac{q\varphi_s}{kT}\right) \tag{4.9}$$

at the semiconductor-insulator interface the normal component of electron and hole current density is identically zero (cf. Fig. 16), hence

$$J_{p_y} = 0;\ J_{n_y} = 0;\quad \frac{d\varphi}{dy} = \text{const} = 0 \tag{4.10}$$

at the left-hand boundary due to symmetry

$$\frac{d\varphi}{dx} = \frac{dn}{dx} = \frac{dp}{dx} = 0 \tag{4.11}$$

In the expressions above the usual symbols have been used: φ is the potential, $J_n(J_p)$ is electron (hole) current density, $\mu_n(\mu_p)$ is electron (hole) mobility, $D_n(D_p)$ is electron (hole) diffusion coefficient, $p(n)$ is hole(electron) concentration, q is an elementary charge, $N_d - N_a$ is net doping concentration, ε is dielectric constant of Si, φ_s is a built-in barrier potential, n_i is intrinsic carrier concentration and $\tau_n(\tau_p)$ is electron (hole) lifetime (relaxation time). We used empirical relations $\mu_{n,p} = F(E, N_d - N_a)$ [26] where E is electric field and Einstein relation

$$\frac{\mu_{n,p} kT}{q} = D_{n,p} \tag{4.12}$$

in our calculations.

Fig. 16 illustrates the solution obtained on a grid with equal space steps along x and y axes (5.0×10^{-8} m), $n_i = 1.5 \times 10^{10}\ \text{cm}^{-3}$, for p-base with doping concentration of $2 \times 10^{15}\ \text{cm}^{-3}$, upper contact width 0.5 µm, $\varphi_s = 0.8$ V, and $\tau_n = \tau_p = 10^{-8}$ s. Equipotential lines in Fig. 17 correspond to the applied voltage of 8 V ($U = \varphi_1 - \varphi_2 = -8$ V). Note that isopotential line for $\varphi = -7.9$ V approximately defines the boundary of the neutral region beyond which the potential changes insignificantly. It is clearly seen from Fig. 16 that near the SiO_2/Si interface a neutral layer exists even for the reverse bias (U) twice as large as a punch-through voltage (U_p). An important conclusion can be drawn from this observation: the absence of the full depletion in p-base is not caused by faulty technological route. The true reason is that the lowest bias required for the full depletion of the SiO_2/Si interface is much larger than U_p. By

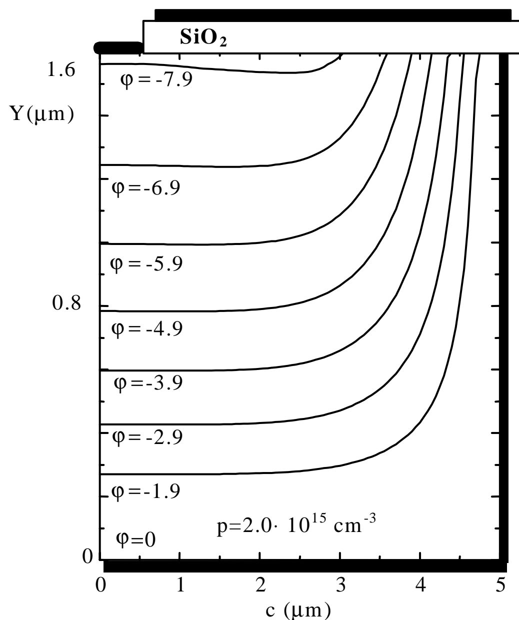

Fig. 16. Equipotential lines in p-base for $U = 2U_p$.

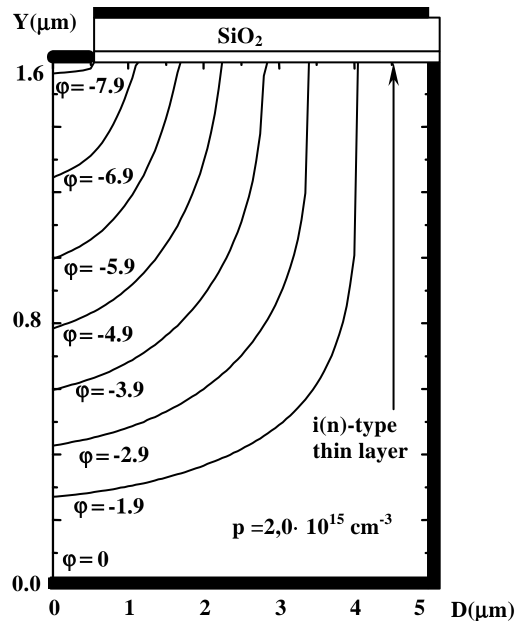

Fig. 17. Equipotential lines in p-base with i-layer inserted beneath the SiO_2 film (all other parameters being identical to that of Fig. 16).

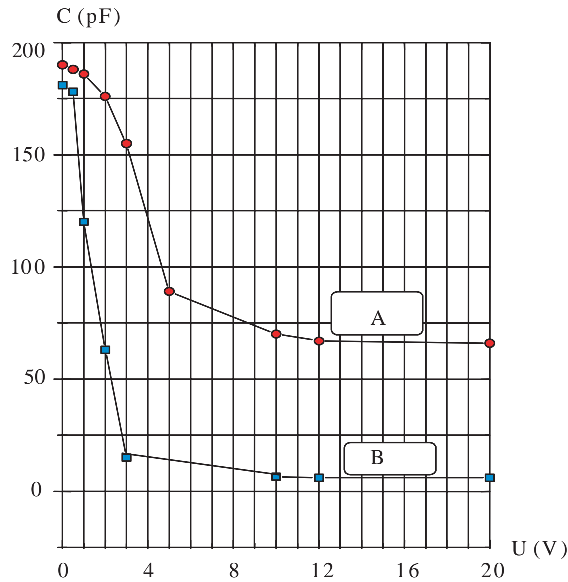

Fig. 18. Comparison of the capacitance–voltage curves measured on SCT without n-layer under the gate (A), and with n-layer in place (B).

extensive numerical work (using simply a trial-and error method) it was found that insertion of a thin n- or i-layer under the SiO_2 film rectifies the situation and allows to achieve full depletion for reverse biases $U \geqslant U_p$. This is illustrated by Fig. 17 where equipotential lines are drawn for exactly the same conditions as in Fig. 16, the only difference being that a layer of i-Si with $n \approx 2 \times 10^{10}\ cm^{-3}$ and a thickness of 5×10^{-8} m was inserted beneath the SiO_2. Numerical results can also be explained in simple terms using only analytical estimates (details may be found in [18,19,25]).

Shown in Fig. 18 are experimental measurements of SCT (between ohmic contact (2) to the active region (1) and gate metallization (4)) for devices *without* (curve A) and *with* (curve B) n-type layer beneath SiO_2. The n-type layer under the gate oxide was fabricated by phosphorus ion implantation (energy 70 keV, dose $1.5 \times 10^{11}\ cm^{-2}$) before thermal oxidation. With n-layer in place, the calculated value of SCT is in satisfying accordance with measured results.

5. Conclusion

Hopefully, in the present article a simple fact has been amply demonstrated: there is a plenty of room in the field of classical semiconductor science and technology, if one is willing to improve existing and to create some new devices without invoking so fashionable recently quantum effects. In any case, it seems useful from time to time to have a fresh look at old things.

Acknowledgments

Over the years many people contributed generously to the work described above, providing their samples, expertise and skills, computer time, money and friendly critique as well as general support. The authors are grateful to all of them. However, without multi-faceted and long-term support to IVM from Askhat Maksutov, Alexander Korenev and Alexander Startsev the mere appearance of almost all ideas and results described in the article would be simply impossible (or, at least, highly problematical). Financial sponsorship to IVM from Vladimir Kolesnikov and Anatoly Lunëv make his life much easier as well as make it possible to perform some experiments. On final stages of manuscript preparation the interaction with Prof. Grigoriy Simin was very helpful. SIC would like to express his special thanks to Dr. Alexander Toropov, Victor Kulman, Dr. Nikolai Korniushkin, Valentina Barkova and last, but not least, Konstantin Svitashev (the late Director of ISP SB RAS). The work of SIC was partially supported by Ministry of Education of Russian Federation within Federal Task Program "Integration" through Novosibirsk State University (Contract No. и0765/785).

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